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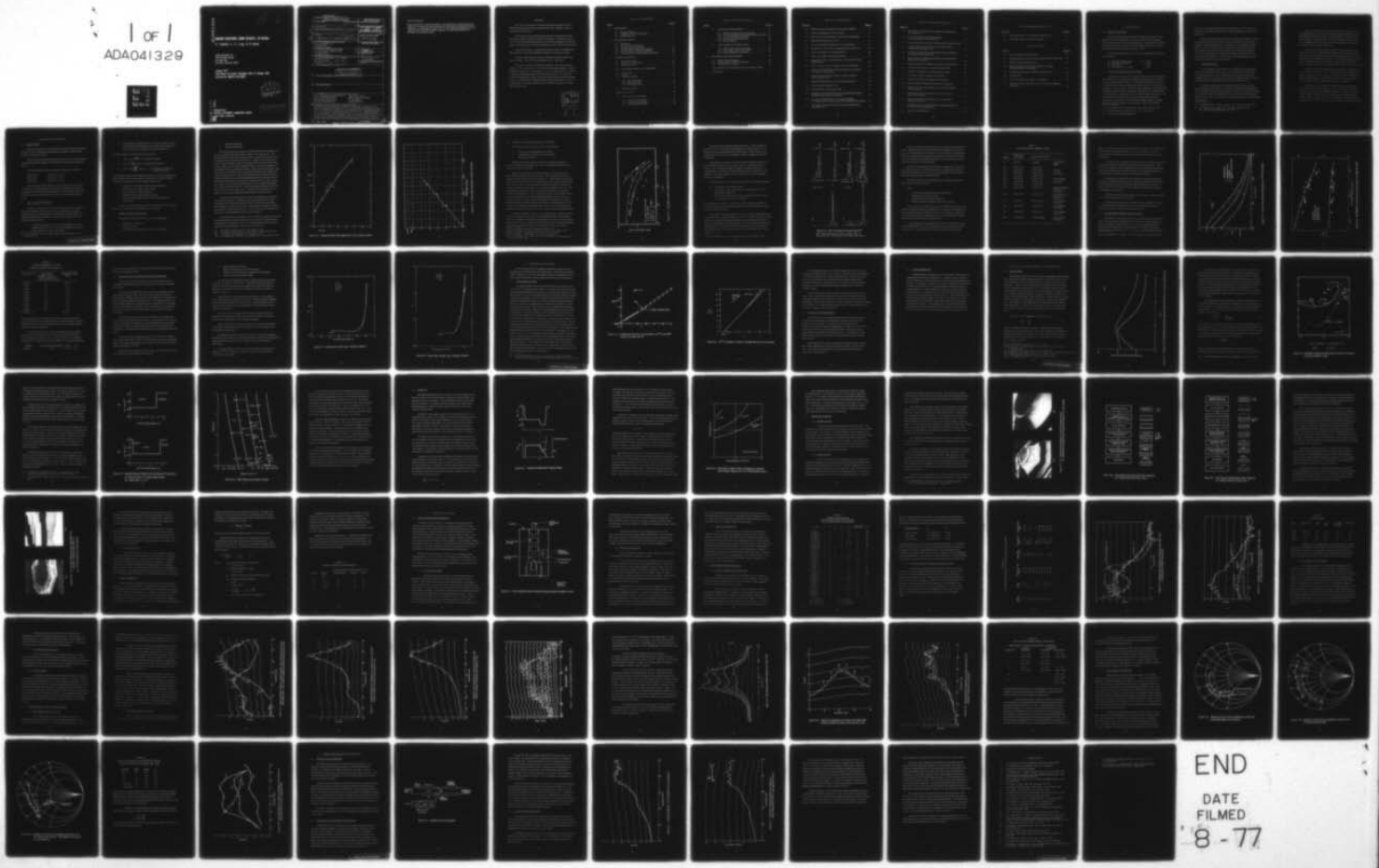

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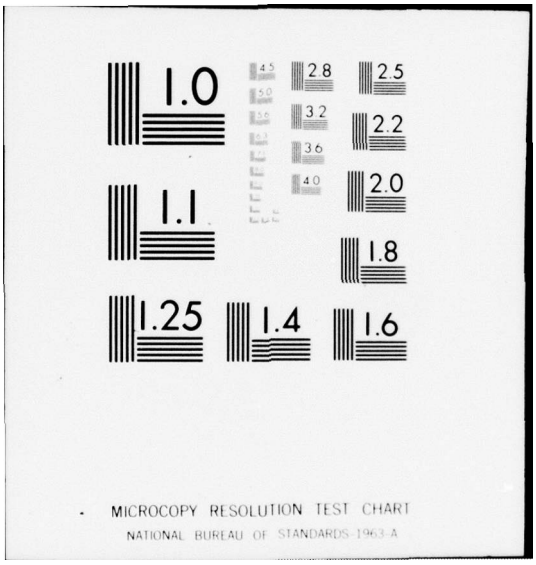
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INDIUM PHOSPHIDE GUNN DEVICES, 26-40 GHz

R. J. Hamilton, Jr., S. I. Long, R. D. Fairman

Varian Associates, Inc.
Solid State West Division
611 Hansen Way
Palo Alto, California 94303

January 1977
Final Report for Period 1 November 1975—31 October 1976
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Prepared for:
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PCl_3, In, H_2 growth process
high effective transit velocity
fast intervalley scattering
longer active regions
Higher frequency limitations
low noise figure
high threshold field

20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

This report covers the period from 1 November 1975 through 31 October 1976 on a research and development program for low noise wideband InP Gunn devices for use in the 26.5 to 40 GHz band. Other performance objectives were: instantaneous bandwidth, 5 GHz; noise figure, 7-9 dB; minimum gain (over 5 GHz), 6 dB. Significant progress has been made in this one-year program in the areas of InP epitaxial growth and material evaluation, device design and fabrication, and test circuit development. It has been verified that InP Gunn devices offer important advantages over GaAs devices in noise

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figure performance as wideband amplifiers. Noise figures up to 13 dB lower than flat profile and 7 dB lower than cathode notch profile GaAs devices have been demonstrated. Additionally, as solid state components, they will offer significant advantages over conventional means of providing wideband, high gain, low noise amplification in the millimeter wave frequency range.

FOREWORD

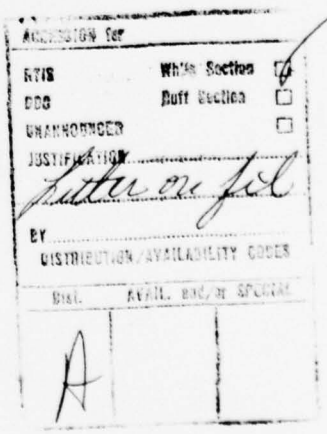
This report is submitted by the Materials and Devices Department of the Solid State West Division of Varian Associates, Palo Alto, California, under Navy contract NOO123-76-C-0265.

In this report, the development and performance of InP Gunn-effect amplifier devices and their associated rf circuitry is described. The frequency range is 26.5 to 40 GHz and amplifier bandwidths of up to 6 GHz are measured in this frequency range. Gain levels of up to 12 dB and noise figures as low as 9 dB have been observed.

These InP Gunn devices, operating at low supply voltages, are intended to be used as high gain, solid state replacement amplifiers for traveling wave tubes.

The work was sponsored by the Naval Electronics Laboratory Center, San Diego, California. The Navy Program Manager was Mr. David Rubin.

This report covers the work begun on November 1, 1975 and completed on October 21, 1976. At Varian, Dr. F. B. Fank was the Program Manager. Principal investigators were Mr. R. J. Hamilton, Jr., Dr. S. I. Long and Mr. R. D. Fairman. In addition to the authors mentioned on the title page, Messrs. T. L. Hierl and J. Andrews supported the program in the area of circuit design and device evaluation. Messrs. S. Lombardi and R. Hendricks performed the major device work. Ms. C. Lowney and Ms. V. Arballo assisted in the area of device work and Ms. T. Miller typed monthly reports.



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1. INTRODUCTION

1.1 PROGRAM OBJECTIVES

The research and development program described in this report is being directed towards the development of low noise, wide band InP Gunn amplifier devices for use in the 26.5 to 40 GHz waveguide band. These efforts were initiated by the Materials and Device R and D Group, Solid State West Division of Varian Associates, Palo Alto, California on November 1, 1975.

The final performance objectives of the devices produced for this program are the following:

(1)	Operating Frequency Range	26.5 - 40 GHz
(2)	Instantaneous Bandwidth	5 GHz
(3)	Noise Figure	7 - 9 dB
(4)	Minimum Gain (over 5 GHz)	6 dB

1.2 ADVANTAGES OF InP FOR GUNN DEVICES

The application of InP for cw transferred electron oscillators and amplifiers in the millimeter wave range provides significant performance improvements over the more widely utilized GaAs devices. In particular, InP is a superior material in several respects. It has a current peak-to-valley ratio of 3.5 as opposed to 2.5 for GaAs [1]. This, in theory, will provide higher oscillator conversion efficiencies. In addition, the peak-to-valley ratio degrades less rapidly with temperature than GaAs and the thermal conductivity is greater, thus favoring cw operation [2]. Due to the high effective transit velocity (1.3×10^7 cm/sec) and fast intervalley scattering [3], longer active regions and higher ultimate frequency limitations should favor InP for millimeter wave applications. Finally, InP reflection

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[1] D.J. Colliver, Proc. 4th Cornell Elect. Eng. Conf., pp 11-20, 1973.

[2] W. Fawcett and G. Hill, Electron. Lett., Vol. 11, pp 80-81.

[3] H. Kroemer, private communication.

amplifiers have demonstrated extremely low noise figures (as low as 7.5 dB) [4], which have been attributed to the lower ratio of electron diffusion to mobility in this material [5].

Another important characteristic of InP is its higher threshold field. Because the threshold field is three times that of GaAs, power densities are much higher. Therefore, thermal limitations under cw operation are more significant, limiting practical cw devices to operation above 18 GHz (where active region lengths are short enough to permit effective heat transfer) or to bias polarities in which the anode is located at the heat sink. Because of the higher electric fields and more critical thermal interactions, cw InP devices are more dependent on bias voltage and current levels than equivalent GaAs devices.

1.3 PROGRESS SUMMARY

From the beginning of this effort, it was recognized that the achievement of the above program goals would require extensive technological advancement in InP materials and device design. During the course of this one-year program, significant progress has been made in the areas of InP epitaxial growth and material evaluation, device design and fabrication, and test circuit development.

Operation of InP Gunn devices in Ka-band requires that thin, uniformly doped, high-purity epitaxial layers be grown under carefully controlled conditions. The understanding and experience gained during the course of this effort has enabled n-type InP active layers with thicknesses in the 4 to 6 μm range and doping levels in the 0.5 to 5.0 x 10^{15} cm^{-3} range to be successfully grown with lower compensation and high purity.

---

[4] S. Baskaran and P.N. Robson, Electron. Lett., Vol. 8, pp 137-138, 1972.

[5] J.E. Sitch and P.N. Robson, Proc. 4th European Microwave Conf., 1974, London: Pitman Publishing, pp 232-236.

Carrier concentration control in this doping range has been successfully accomplished using both H_2S and mole fraction (si) dopants yielding flat profiles. Sulfur-doped buffer layers have been evaluated and found to be useful in minimizing the incidence of high resistivity regions at the substrate-active layer interface. Techniques have been developed to predict and maintain moderate growth rates under a variety of operating conditions.

Concurrently, material evaluation methods have been modified and optimized for use on n-InP. Evaporated gold Schottky barriers have been effectively utilized at reduced temperatures to accurately measure doping profiles. Van der Pauw specimens were prepared to determine carrier mobility and impurity compensation. Photoluminescence measurements were used to monitor the presence or absence of acceptor levels (Zn, Hg) contributed by the indium metal or quartz hardware.

Existing contacting technology employing dc sputtered Au-Ge/Ni films was used in preparing device chips. Ohmic contacts with low series resistance were obtained. Conventional scribe and cleave and ultrasonic bonding techniques were utilized during the program to obtain initial dc and rf results on packaged devices while gold plated integral heat sink modifications were investigated.

A total of three rf test circuits were designed, fabricated and tested to assist in the evaluation of Ka-band diodes. All were of the coaxial-waveguide hybrid type and were centered at different frequencies in the band. A wide range of center conductors and heat sinks were utilized to provide optimum circuit conditions. Gains as high as 8 dB over 5 GHz bandwidths and noise figures in the 9-11 dB range in wideband, slightly lower gain (4-6 dB) circuits have been observed.

2. InP EPITAXIAL GROWTH

2.1 INTRODUCTION

The PCl_3 In, H_2 process has been selected as a process capable of producing epitaxial InP layers of high quality, high purity for fabrication of Gunn amplifier devices for Ka-band (26-40 GHz).

The basic PCl_3 process first described by Clarke et al [6] has been developed into a practical operation suitable for the preparation of high quality epitaxial InP layers.

The materials specifications for the Ka-band amplifier are as follows:

Contact Layer:	1-2e17 cm^{-3} x 0.5 μm
Active Layer:	1-2e15 cm^{-3} x 4-5 μm
Buffer Layer:	1-2e17 cm^{-3} x 1-2 μm

In the initial stages of the contract, a study of the basic process variables as related to the electrical and physical properties of epitaxial InP was required. An investigation of the fundamental relationships concerning epitaxial layer purity and growth rate is the key to control of the process for device quality epitaxial layers.

2.2 PCl_3, In, H_2 GROWTH PROCESS

The PCl_3, In, H_2 process provides the most direct approach to high purity InP growth available. The system involves the smallest number of chemical components along with the highest purity of phosphorous and HCl combined. The chemical transport from a phosphorus saturated In source includes two unique impurity segregation effects:

1. A liquid/solid segregation coefficient which inhibits the transfer of impurities found in the In source by their segregation from the InP crust covering the In source at equilibrium.

[6] R. C. Clarke, B. D. Joyce, W. H. E. Wilgor, Solid State Commun., vol 8, pp 1125-8, 1970.

2. A thermodynamic equilibrium between the group IV impurities and the free HCl present in the deposition stage inhibits dopant incorporation at the growth site from any group IV impurity halide present.

The major reactions for the PCl_3 process are as follows:

1. $4\ PCl_3 + 6\ H_2 \xrightarrow{500°C} P_4 + 12\ HCl$ (PCl_3 reduction)

2. $4\ In + P_4 \xrightarrow{750°C} 4\ InP_x$ ($x < 1$) (phosphorous saturation)

3. $4\ InP + 4\ HCl \underset{650°C}{\overset{750°C}{\rightleftharpoons}} 4\ InCl + P_4 + 2\ H_2$ (fundamental transport and deposition reaction)

The similarities between the well studied $AsCl_3$ process and the PCl_3 technique are great and therefore allow greater depth to be undertaken in the latter technique. The following similarities have been documented and observed:

1. Dependence of layer doping on metal source temperature
2. Indium saturation and III-V crust formation
3. PCl_3 mole fraction control techniques
4. High purity H_2 and reactor integrity methods
5. Optimum reactor design for the growth of uniform doping and film thickness

Using the technical knowledge gained with 10 years' experience in the $AsCl_3$ process, many of the pitfalls in InP epitaxy have been avoided.

2.3 PHYSICAL PROCESS DEPENDENCES

The epitaxial growth rate in the PCl_3 process is dependent upon:

1. Indium source temperature
2. PCl_3 mole fraction
3. Mass transport effects (with constant PCl_3 mole fraction)

4. Substrate temperature

5. Thermal profile effects

The thermodynamics of the reaction of InP with HCl have been studied [7,8]. The results indicate a first order reaction similar to the $AsCl_3$ case [9]. The epitaxial growth rate of the PCl_3 process as shown in Figure 2.1 illustrates a power law proportionality with the PCl_3 mole fraction. A change of 10X in the PCl_3 mole fraction, which is defined by moles of PCl_3 divided by the sum of the moles of PCl_3 and H_2, results in a three order of magnitude change in net carrier concentration. Any change in the PCl_3 concentration results in a direct change in growth rate. The $AsCl_3$ process has been shown to be free of growth rate changes over factors of 3X in $AsCl_3$ concentration [10]. The mass transport effects are evident in Figure 2.2 where mass transport (flow rate) is plotted against growth rate showing a linear relationship, characteristic of mass transport limited processes (e.g. $SiCl_4$, $GeCl_4$, etc). Again, the $AsCl_3$ process has been shown to be free of growth rate changes over a factor of 6X in flow rate [10]. Both of these effects predominate in the control of growth rate by the PCl_3 process. Excessive In source temperature play a minor role in growth rate enhancement and contribute to higher net doping.

The shape of the thermal profile is critical to the stability and maintenance of the InP crust formation. Gradients in the In source region lead to less than complete InP crust formation and permit the loss of crust under marginal PCl_3 input conditions. As in the $AsCl_3$ process, adequate group V saturation is an absolute necessity in maintaining the In/P ratio. Once the InP crust is established, the In/P ratio is fixed throughout the entire deposition sequence.

Thermal profiles in the deposition region are critical for uniform layer growth. Graded thermal profiles produce nonuniform layers due to the exponential growth rate impedance on temperature. Our work with flat deposition profiles has shown uniform layer growth similar to the $AsCl_3$ case (see Section 2.5).

[7] D.W. Shaw, J. Phys. Chem. Sol. vol 36, pp 11-8, 1975.
[8] H. Seki and S. Miragawa, Jap. J. Appl. Phys., vol 11, pp 850-4, 1972.
[9] D.W. Shaw, J. Crys. Growth, vol 8, pp 117-128, 1971.
[10] R. Fairman and R. Soloman, J. Electrochem. Soc. vol 120, pp 531-4, 1973.

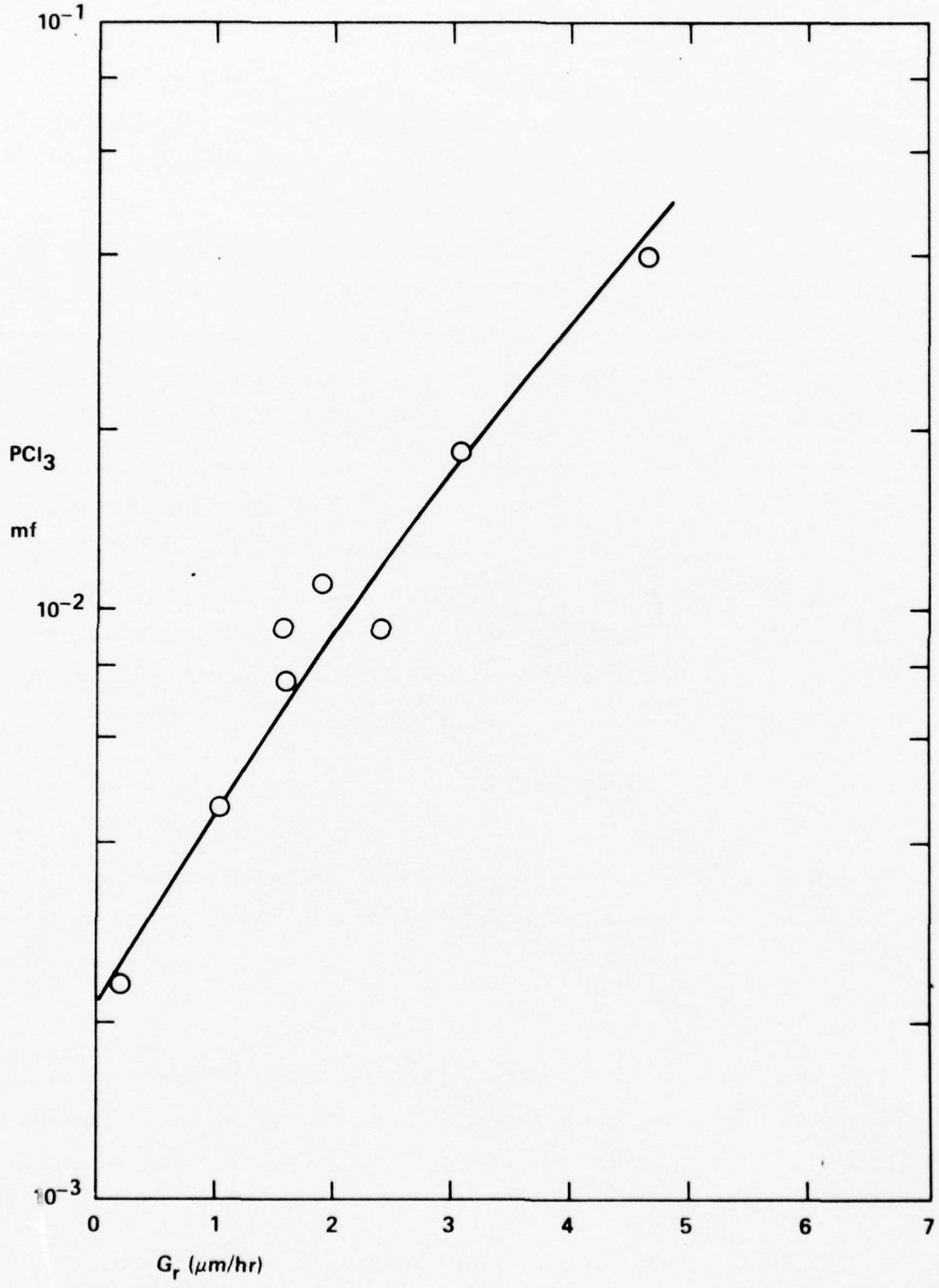

Figure 2.1. Epitaxial Growth Rate Dependence of PCl_3 Molar Fraction

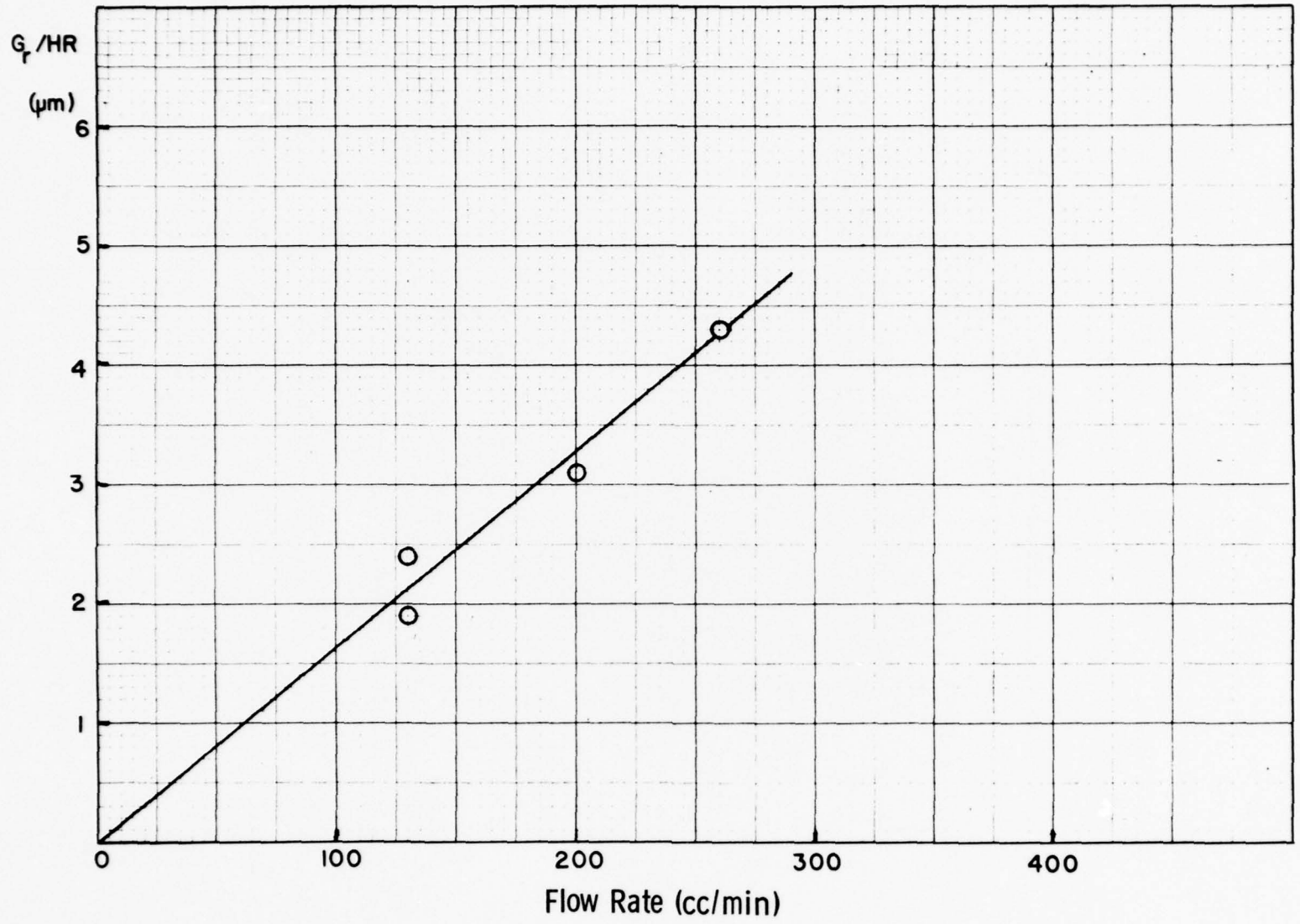

Figure 2.2. Growth Rate Dependence of Mass Transport

2.4 VARIABLES AFFECTING ELECTRICAL PROPERTIES

Net doping and purity are influenced by the following factors.

1. PCl_3 mole fraction dependence of net doping.
2. H_2S backdoping and effects of PCl_3 mole fraction.
3. Foreign impurity effects

The PCl_3 mole fraction effect on net carrier concentration reported by Clarke [11] shows a major change in net carrier concentration produced by minor changes in the PCl_3 mole fraction.

Figure 2.3 shows PCl_3 mole fraction dependence. Data from Clarke are shown along with data from two Varian reactors. The PCl_3 mole fraction effect is similar to that encountered in the $AsCl_3$ process [12]. The mechanism for the $AsCl_3$ mole fraction effect is believed to be a thermodynamic one involving the generation of chlorosilanes from HCl reactions with quartz at high temperatures and subsequent interaction with HCl concentrations at lower deposition temperatures [13, 14]. This thermodynamic argument also applies to other group IV impurities and has been observed experimentally [15]. It is postulated here that the same residual impurity, Si, is also responsible for the background doping dependence observed in the PCl_3 mole fraction effect. The mole fraction method interacts with all of the available impurities present and should only be used for doping concentrations that are several times the normal minimum background doping. However, the best uncompensated epitaxial material grown to date has been grown using the mole fraction doping control.

Backdoping with H_2S is a much more controllable process, as the major doping is set by accurately limiting the H_2S concentration with mass flow control systems. Under these conditions, the background doping should be less than 10% of the intended doping in order to be free of variable background doping effects. Remote programming of epitaxial layer doping can easily be accomplished as was done in VPE GaAs.

[11] R. C. Clarke, J. Crys. Growth, vol 23, pp 166-8, 1974.
[12] B. Cairns and R. Fairman, J. Electrochem. Soc. vol 15, pp 327C, 1968.
[13] J. V. Di Lorenzo, J. Crystal Growth, vol 17, pp 189-206, 1972.
[14] M. E. Weiner, J. Electrochem. Soc. vol 119, pp 496, 1972.
[15] J. V. Di Lorenzo, G. E. Moore, Jr. and A. E. Machala, J. Electrochem. Soc, vol 117, pp 102C, 1970.

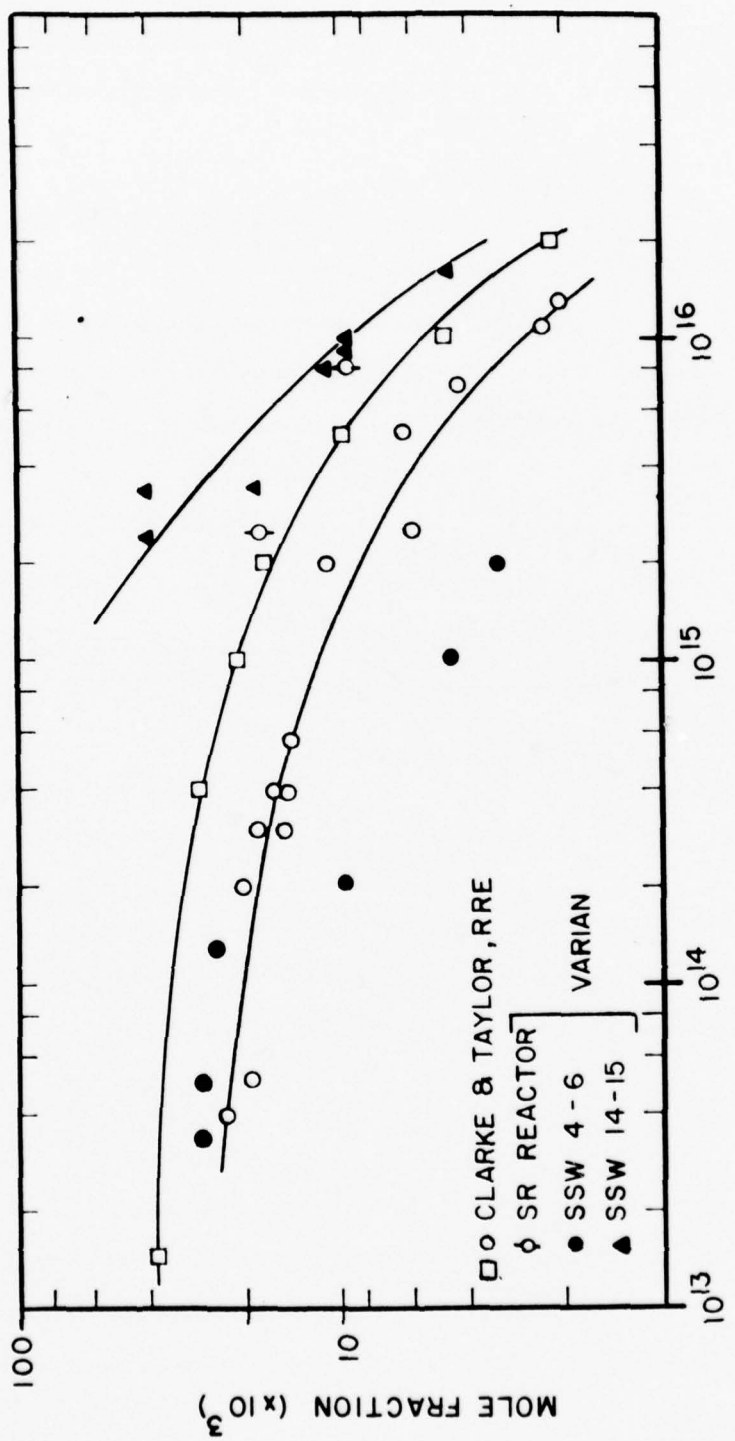

Figure 2.3. PCl_3 Molar Fraction Dependence of Net Carrier Concentration

The major foreign impurities present are Zn and O_2. Other workers have observed Cd, Hg, Cu, Bi and Mn by photoluminescence measurements at 2°K [16]. In the present work, photoluminescence measurements are made routinely on all VPE InP layers at 77°K in order to evaluate the relative Zn impurity concentration in these films.

At this point in our work, we have experienced two different sources of Zn. The 99.9999% purity In metal from Cominco, Alusuisse, Mining and Chemical Products, Ltd., and Johnson-Matthey all contain trace (ppb) quantities of Zn. A composite figure (2.4) shows the measured photoluminescence emission due to Zn impurities. The Johnson-Matthey Grade A-1 In is the only source of In available with low Zn concentration.

In our initial work, the 6-9s In metal was purified by the following technique:

1. Air oxidation to form impurity oxides
2. Decanting the molten In away from the resultant oxides into a carefully purified graphite boat
3. Hydrogen firing at 900°C for 72 hours in UHP H_2 to remove dissolved O_2, residual In_2O_3 and Zn by evaporation

The resultant In was loaded into a VPE reactor, while contained in a Spectro-sil quartz boat, and fired again overnight to remove oxides formed during the transfer of the pure metal to the reactor.

The results of this purification are shown in the composite photoluminescence scans of Figure 2.4. Additional quantities of Zn were encountered later from a quartz reactor tube which had been contaminated with Zn during fabrication in the glass shop. By eliminating the contaminated quartz, the Zn level returned to the previous background level. Hg is often observed in the photoluminescence spectra of the first deposition from a new 6-9 In source, but is no longer detected by the second deposition.

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[16] E. W. Williams et. al., J. Electrochem. Soc. vol 120, pp 1741, 1973.

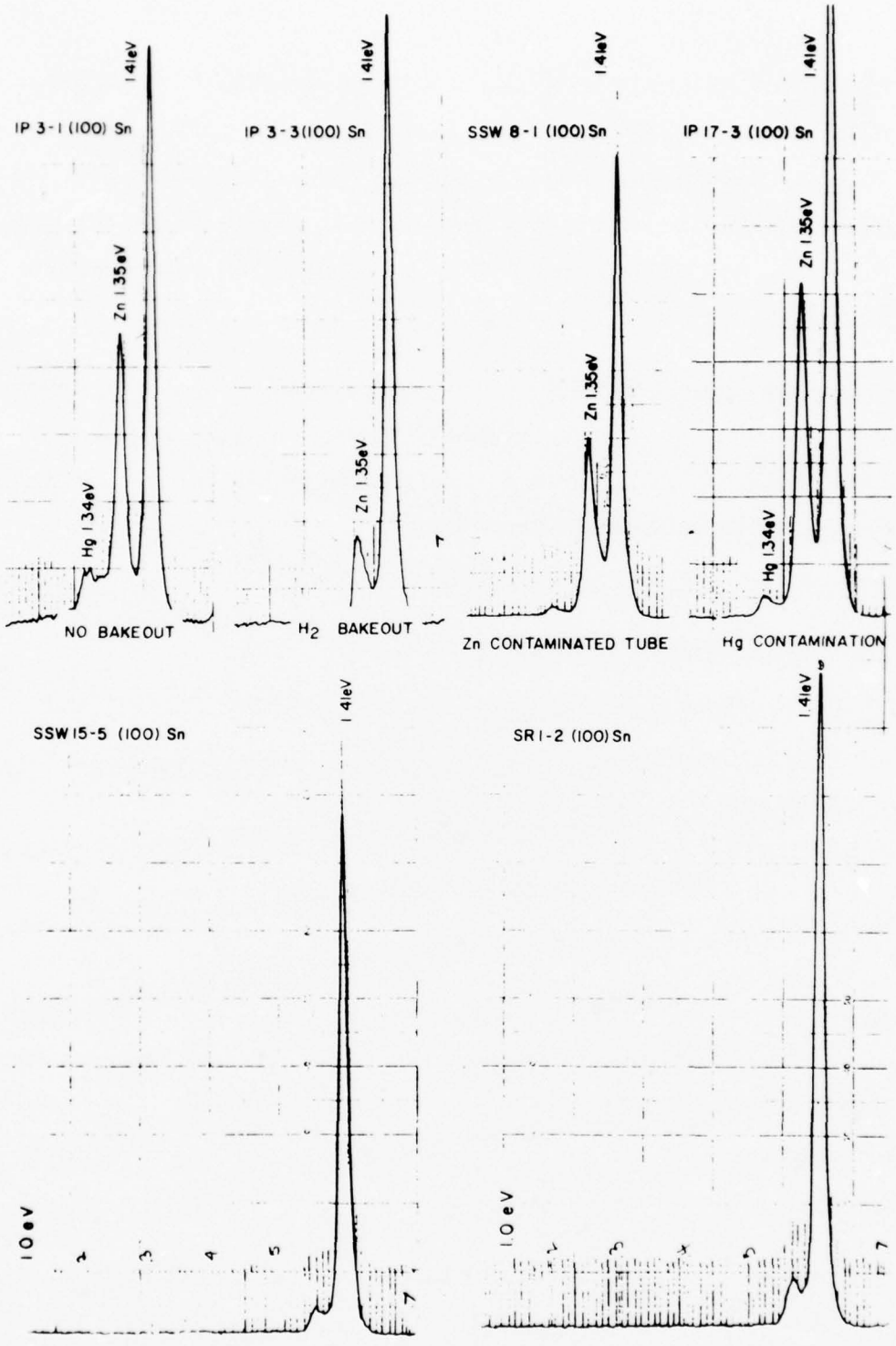

Figure 2.4. VPE InP Photoluminescence at 77°K

(The vertical scale represents linear intensity. The two bottom spectra are measurements made on high purity indium.)

Oxygen is a deep-level impurity that cannot be detected by photoluminescence at 77°K. Subsequent effort has been directed towards capacitance decay measurements in order to establish the true energy level and concentration in compensated InP layers. Infrared measurements of air-exposed PCl_3 sources showed evidence of $POCl_3$ formation, which exhibits approximately 1/4 of the total vapor pressure and therefore cannot be removed by purging.

Since the air contaminated PCl_3 had become a constant source of O_2 doping, a gas-tight N_2 glove box was used to eliminate the O_2 contamination encountered during the PCl_3 transfer, and a gate valve is being designed to reduce the reactor contamination during substrate loading operations.

An analysis of the deep level contaminants was made using Van der Pauw Hall mobility of the following samples.

Type:

1. Early runs with Alusuisse 6-9s In and O_2 doped PCl_3
2. Alusuisse 6-9s In and O_2 free PCl_3
3. Johnson-Matthey 6-9s In and O_2 free PCl_3
4. Mining and Chemical Products 6-9s In and O_2 free PCl_3

Table 2.1 shows the complete carrier freeze-out effects at 77° K for type (1) samples containing the greatest concentration of O_2. Type (2) and (3) samples with different In purities indicate a different degree of carrier freeze-out. Other deep level impurities not detected by photoluminescence or mass spectroscopy could be responsible for the minor freeze-out effects at 77°K.

A major distinction in the resultant InP layer purity as related to the source of high purity In metal can be seen by plotting free carrier concentration vs Hall mobility at 77°K. A comparison with calculated compensation curves by Rode

Table 2.1

VAN DER PAUW HALL MOBILITY VPE InP

Sample	$\mu_{H300}/\mu_{H77°\,K}$ (cm^2/v-sec)	N_D-N_A 300/77°K (cm^{-3})	
6-2	5480/NA	1.7e14/NA	Alusuisse 6-9s indium
11-1	5470/42,000	5.1e15/.1e15	
11-2	4760/37,720	1.7e15/5.2e14	Alusuisse
11-3	3900/23,550	1.9e16/3.7e15	6-9s indium
14-1	4140/20,870	1.49e16/1.1e16	
14-2	4980/25,660	8.6e15/7.0e15	Johnson-Matthey
14-3	4670/36,470	2.7e15/2.4e15	6-9s indium
14-4	4370/37,570	2.2e15/1.9e15	
17-1	6060/140,220	1.2e13/1.3e13	Mining and Chemical Products, Ltd. 6-9s indium
17-3	5180/73,950	5.8e14/5.5e14	Mining and Chemical Products, Ltd. 6-9s indium
22-1	4620/54,480	1.45e15/1.33e15	Johnson-Matthey 6-9s indium
32-2	4850/89,100	6.6e14/6.8e14	Johnson-Matthey 6-9s indium
32-3	4630/61,090	8.9e14/7.3e14	Johnson-Matthey 6-9s indium
SR7-1	4700/60,050	1.58e15/1.69e15	Johnson-Matthey 6-9s indium

(Figure 2.5) shows the highest purity In (Johnson-Matthey) to fit a 1.25:1 compensation curve and type 2 In (Alusuisse) fitting a 2:1 compensation model. The family of curves are lines of constant total impurity concentration divided by net free carrier concentration.

As a result of lower compensation with type (3) In, the net carrier concentration has increased an order of magnitude for the same PCl_3 mole fraction used. This increase in net doping is real and responsible for the lack of deep level compensation. A good agreement has been shown between the PCl_3 mole fraction-net doping for two VPE InP reactors using the same purity constituents as in Figure 2.3.

The dependence of doping efficiency on substrate temperature appears to be a second order effect based upon preliminary experiments in the range of 620-660°C. Additional effort will be taken to reduce the background doping of the system to a maximum of 10^{14} cm^{-3} to allow the growth of lightly doped layers and to assist in the backdoping control with H_2S.

A summary of the high purity InP data is shown in Figure 2.6 as Hall mobility vs net carrier concentration for 300 and 77°K.

Epitaxial film doping uniformity was measured on sample SSW.15-2 in order to characterize the present epitaxial process. The net doping measured by C-V methods at 77°K has been reduced and is shown in Table 2.2.

2.5 MASS TRANSPORT LIMITED GROWTH EFFECTS

Recent data [17] have shown the PCl_3, In, H_2 process to be mass transport limited. The PCl_3 mole fraction dependence of growth rate is shown in Figure 2.1. These gross changes in epitaxial growth rate for InP have suggested other than kinetic growth rate limitations. Experiments with constant PCl_3 mole fraction, substrate and source temperatures have shown a linear relationship between growth

[17] R. C. Clarke and L. L. Taylor, J. Crystal Growth, vol 31, pp 190-6, 1976.

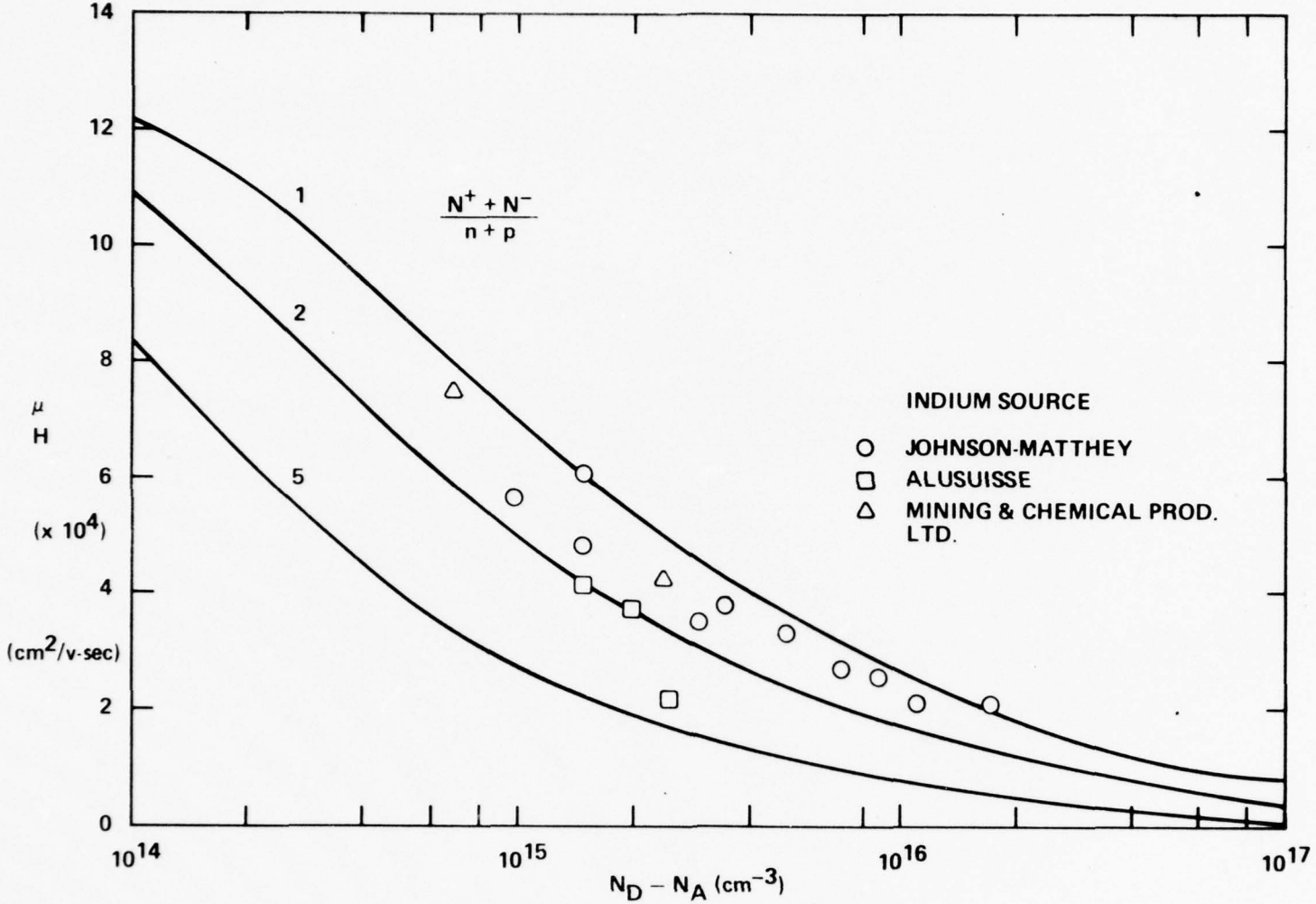

Figure 2.5. Carrier Concentration Dependence of 77°K Hall Mobility

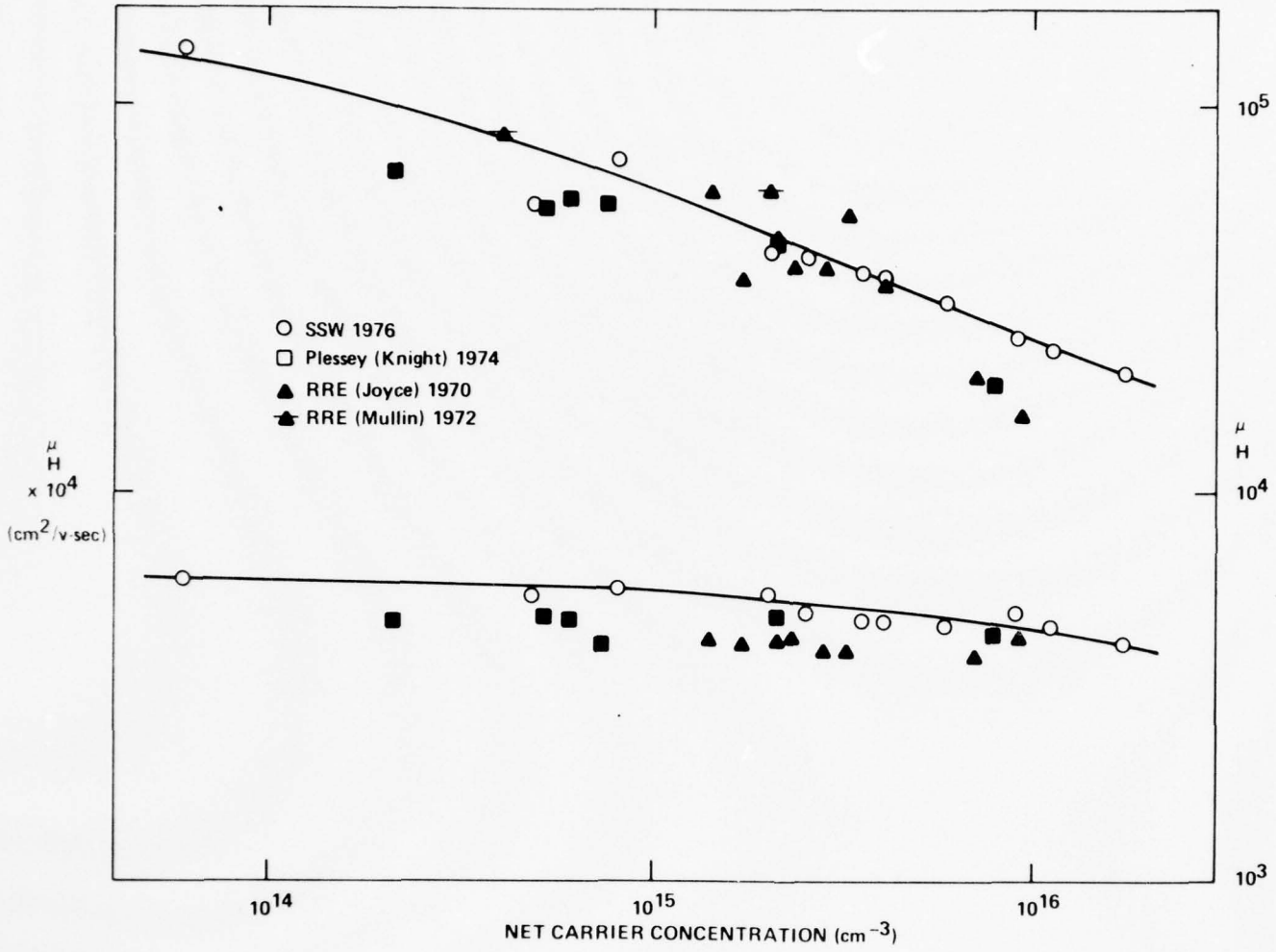

Figure 2.6. Hall Mobility vs Net Carrier Concentration for 300°K and 77°K

Table 2.2

DOPING UNIFORMITY, PCl_3 MOLE FRACTION CONTROL SSW 15-2 (100), n/n^+

Avg N_D-N_A (cm^{-3})	Diode Location (Evaluation donuts are located in a square grid pattern with 0.080" centers)	Uniformity in Doping Profile %
9.95e15	2,5	±7.6%
1.10e16	2,9	5.8%
1.01e16	3,2	4.6%
1.12e16	4,5	5.8%
9.75e15	7,2	2.8%
9.60e15	7,9	4.6%
1.15e16	9,6	4.0%
1.10e16	10,12	3.6%
9.20e15	11,1	6.0%
1.08e16	12,3	3.4%
avg. 1.05e16 ± 7.5%		avg. 4.8%

rate and mass transport for (100) InP. The control of absolute growth rate is extremely critical for the reproducible preparation of layers suitable for Ka-band amplifiers; the addition of mass transport limited growth rate adds an essential dimension of control to the process.

The uniform thermal profile requirements sought for control of uniform growth rate across the substrate can be evaluated by epitaxial film thickness measurements in the direction of gas flow. The ΔT across a 1-2 cm substrate is less than 0.5°C. Measurements of sample SSW15-2 have revealed the following:

SAMPLE	AVG LAYER THICKNESS (μm)	σ (μm)	σ %
SSW15-2	5.55 μm	± 0.23 μm	± 4.1%

The above data fit well with the 3-5% variations observed in the GaAs VPE process using the same flat profile method.

2.6 GROWTH OF ACTIVE DEVICE STRUCTURES AND CONTACTS

The study of basic process variables has allowed the growth of uniform, device quality epitaxial films that are now relatively free of traps and crystalline imperfections.

A comparison of backdoping techniques with PCl_3 mole fraction control vs vapor doping with H_2S was made. The mole fraction control method utilizes a thermodynamic mechanism which controls the halide stability at the crystal growth site. It regulates the doping by interacting with all of the impurities present. If the predominant impurity is an acceptor which has a stable halide, it will regulate the net acceptor doping as well as the net donor concentration in an n type system. In the PCl_3, In, H_2 process the residual dopant is Si from the quartz reactor construction.

The N_D/N_A ratio vs the trichloride mole fraction is not a constant in the GaAs process and most likely is not in the PCl_3, In, H_2 system as well. By fixing the PCl_3 mole fraction and introducing a vapor dopant such as H_2S, the acceptor concentration remains at a minimum and greater control can be achieved over compensation. The heavily doped contacts are also more easily produced with vapor doping.

The growth of uniform impurity profiles at $> 10^{15}$ cm^{-3} can be attained by either approach while those $< 10^{14}$ cm^{-3} require greater control of the background doping. Autodoping from the buffer layer is a major deterrent to the mole fraction method when growing $< 10^{15}$ cm^{-3}.

Problems associated with i layers at the substrate epi layer interface early in the program have been attributed to the following:

1. Surface impurity ion diffusion
2. Structural imperfections of the interface region
3. Diffusion of foreign impurities originating from the substrate
4. Vacancy effects of the interface region.

All of the previous difficulties have been completely resolved by the growth of a buffer layer doped to 1-2 x 10^{17} cm^{-3}. When lightly doped active layers are grown, the exact doping parameters for the buffer layer become more critical in InP growth. An example of the active layer-buffer layer interface is shown in Figures 2.7 and 2.8.

Notch profiles have been approached with this system. The results have shown a doping spike at the buffer layer-active layer interface caused by inadequate control over vapor etching between the two layers. Additional equipment will be required to solve this problem and its installation will be delayed into the remaining portion of the contract.

Our recent work involving the control of background inpurity levels has allowed the use of higher PCl_3 molar fractions which are essential in permitting the control and reproducibility of low, intentional backdoping.

Much of the success in reducing the acceptor levels was due to the reduction of residual Zn in the indium source and elimination of O_2 of a contaminant in the PCl_3 and indium metal source.

The fitting of recent Hall mobility data to Figure 2.5 (Carrier concentration dependence of Hall mobility at 77° K by Rode) illustrates the extension of uncompensated epitaxial growth down to mid-10^{14} levels without increasing the compensation ratio (1.25:1).

The major portion of our work will involve the further development of low doped ($< 3 \times 10^{14}$ cm^{-3}) triple layer structures with closely controlled lengths and maximum contact doping.

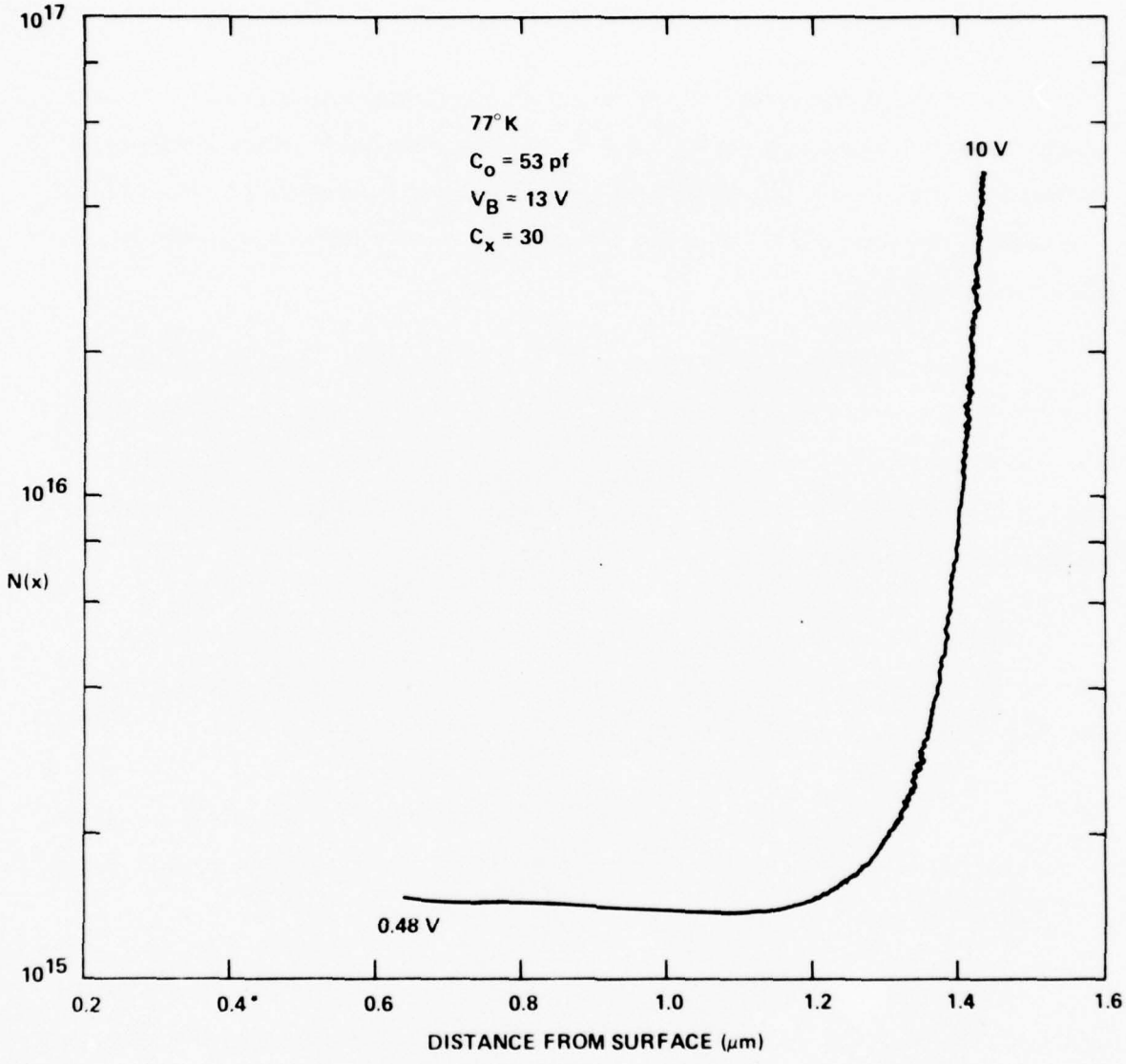

Figure 2.7. Active Layer-Buffer Layer Interface SSW21-3

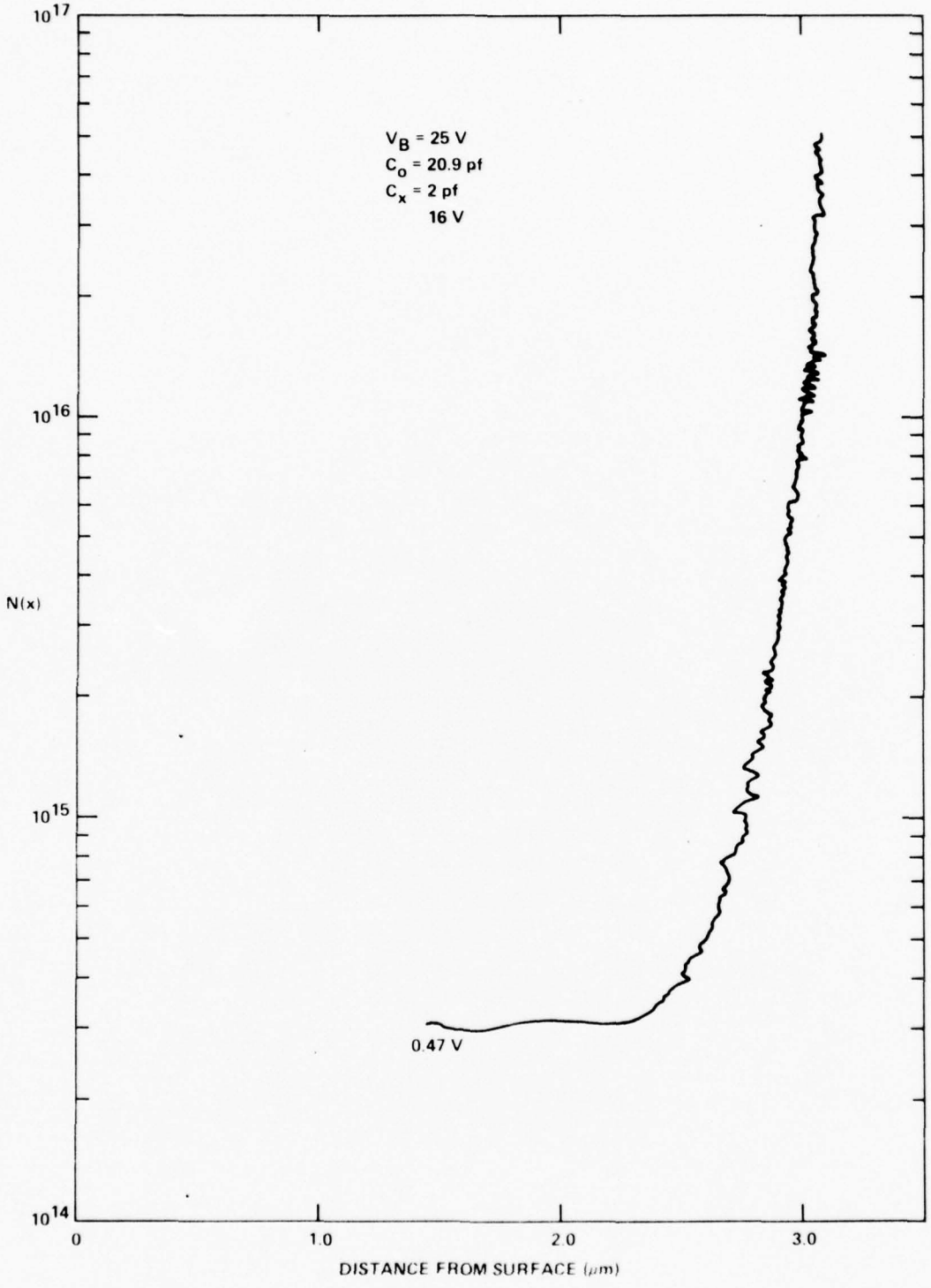

Figure 2.8. Active Layer-Buffer Layer Interface SSW27-3

3. MATERIAL EVALUATION

The InP layers grown were evaluated by capacitance voltage (C-V), Van der Pauw, and photoluminescence (PL) measurements. The carrier concentration profile is obtained from C-V data, the mobility and carrier concentration from the Van der Pauw measurement, and the impurity levels from the PL measurement.

3.1 CAPACITANCE VOLTAGE

The built-in potential of the Au-InP Schottky barriers was determined to be 0.23 eV by C^{-2} vs V plot as shown in Figure 3.1. Because of the low barrier height for the metal to InP Schottky barrier junction, only p and n layers doped in the range of less than 10^{15} have been successfully probed by reverse bias capacitance measurement at room temperature. One way to circumvent this problem is to use a metal-insulator semiconductor structure [18] instead of a metal semiconductor junction. However, for the mm-wave applications, the required device thickness is small, and growing and removal of a thin oxide layer on the semiconductor is undesirable as well as time consuming. Instead, the Au InP Schottky barrier system was used to obtain the C-V data at 77°K. Because of the low temperature, the reverse leakage current of the junction is low enough to make the C-V measurement. In order to check out the validity of the low temperature measurement, the same junction was measured on a modified Boonton capacitance bridge at room temperature. With the modification of the bridge, the leakage current of a device can be tolerated down to Q = 1 (real part equal to reactive part of the diode impedance). From a typical Au-InP Schottky diode, the Q of the device varies around 1 from V = 0 to about 0.2 V, and is above 1 from V = 0.3 V up to almost breakdown voltage. InP wafers which did not show any carrier freeze-out showed the carrier concentrations taken at room and the liquid nitrogen temperatures to be identical within limits of measurement error as indicated in Figure 3.2. This indicates that the dominant carrier density occurs with shallow states and with very little deep level compensation, which is representative of high quality epitaxial InP. The same behavior was obtained from both wafers grown by either mole fraction or S doping control.

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[18] M.J. Caldwell and R.F. Peart, "Measurement of Carrier-Concentration profiles in epitaxial indium phosphide," Electronics letters vol 9, pp 88-89, 1973.

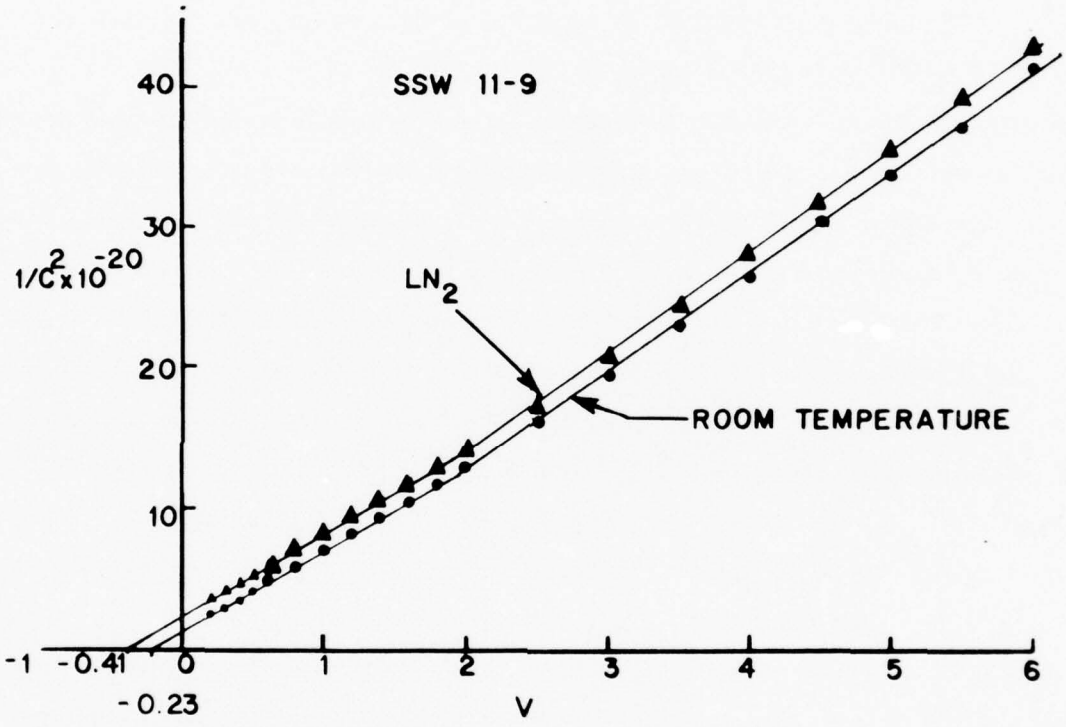

Figure 3.1. Comparison of Carrier Concentrations at 77°K and 300°K using Au Schottky Barrier

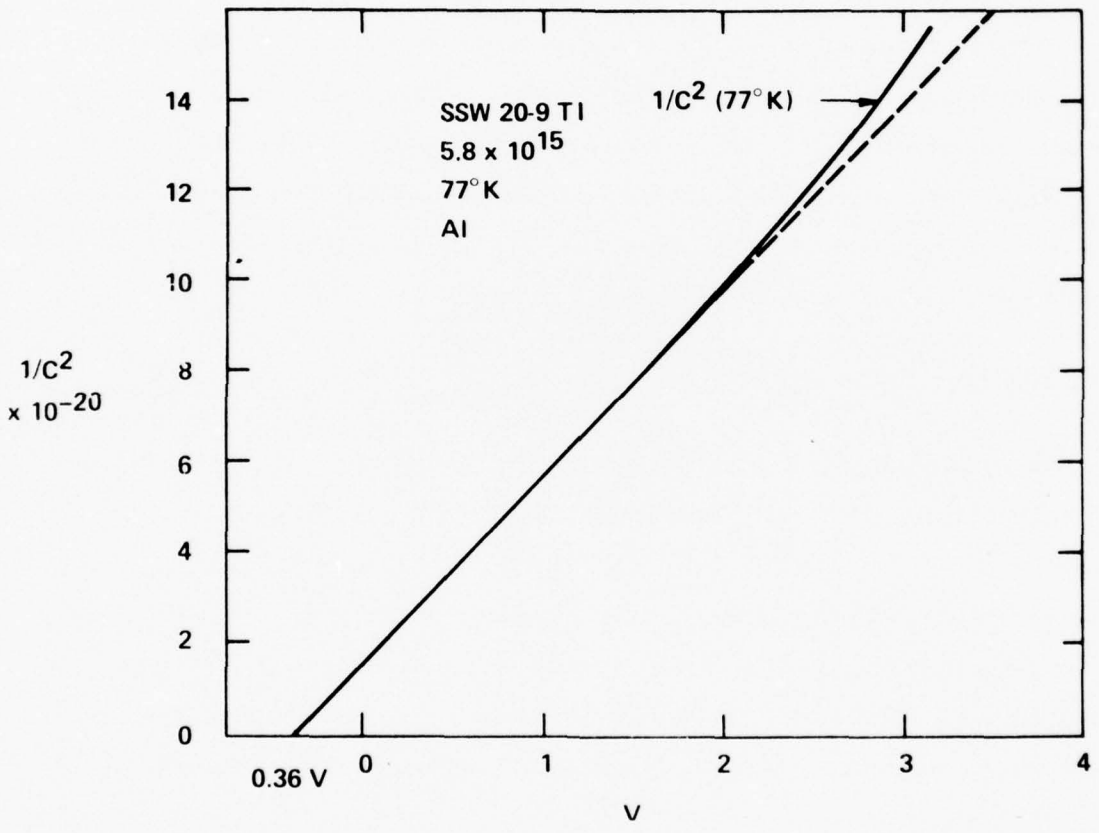

Figure 3.2. $1/C^2$ vs Voltage of a Good Al Schottky Barrier on InP Surface

The Au Schottky barriers used for wafer evaluation have shown some signs of intermetallic diffusion in InP. When a previously evaporated chip is first stripped of Au, the wafer surface shows no real preferential etching. After the same wafer is etched in a Br-methanol etch, the Schottky barrier pattern reappears due to preferential etching of the contacted areas. The Au evaporation employs substrate temperatures < 200°C, but preferential heating by radiation could well affect the metallized regions.

Because of the above problem, aluminum was chosen as alternate barrier metal. It has yielded a barrier height nearly as good as Au when processed in our ion pumped evaporator. The Al barriers were later removed with the commercial gold stripper, with excellent results and no evidence of diffusion or preferential etching. The Al barriers were evaluated by measuring the built-in voltage as determined from $1/C^2$ plots of voltage as shown in Figure 3.2.

3.2 VAN DER PAUW MEASUREMENT

The carrier freeze-out was detected by the Van der Pauw measurement as well as the C-V measurement. Tin and AuGeNi contacts were used on a clover shaped Van der Pauw sample. Tin contacts were used for thick sample evaluation and the AuGeNi contacts for thin samples. In Table 2.1 the Van der Pauw data are presented for runs with two different In sources, indicating a basic In purity difference which relates to carrier freeze-out. As was expected, devices fabricated from the wafer which showed the carrier freeze-out did not work well in the cw mode.

Some difficulties were observed in measuring samples less than 3 μm thick due to built-in depletion layers from surface and/or substrate active layer interfaces. This effect was circumvented by growing samples thicker than 3μm to reduce the measurement error.

3.3 PHOTOLUMINESCENCE

Photoluminescence measurements at 77°K were used for routine screening of epitaxial films for shallow acceptor levels. A chopped Ar laser was used to excite the states and a cooled S-1 detector was used to detect the photoluminescence emission. This technique is sensitive only to acceptor conduction band transitions with energy greater than 1.0 eV. The main impurity level observed from this measurement was Zn. The incorporation of Zn has been correlated with the In purity parameters. An example of spectra as a function of growth parameters (in this case, purity of In metal) is shown in Figure 2.4. Wafers exhibiting carrier freeze-out at 77°K cannot be used for cw devices. The shallow Zn level is not responsible for carrier freeze-out. Other undetermined deep level (or levels) is causing the freeze-out. A wafer suitable for cw device operation showed no significant acceptor (Zn) levels from the PL measurement and minimal carrier freeze-out as shown by C-V measurements made at room temperature and 77°K.

4. 26.5-40 GHz DEVICE DESIGN AND FABRICATION

4.1 DEVICE DESIGN

The utilization of InP for cw transferred electron amplifiers in the millimeter wave region has demonstrated significant performance improvements over the more widely utilized GaAs devices. In particular, InP is a superior material for this application. Figure 4.1 shows a theoretically generated plot of hot electron diffusivity as a function of electric field [19, 20]. The diffusion coefficient D for InP is considerably less than that of GaAs at electric fields in the 1.5-2 times threshold range. Since the diffusion coefficient is a measure of statistical variation in the electron velocity, high diffusion results in high noise. This low diffusion coefficient in InP is a consequence of strong polar and intervalley scattering above threshold [21]. From Figure 4.1 it is evident that for both materials, the region around threshold should be avoided for low noise operation. This is a consequence of the random nature of intervalley scattering which predominates about the threshold field.

A qualitative noise temperature can be defined by [22].

$$\frac{kT}{q} \approx \frac{D}{|\mu|} \qquad (1)$$

where μ is the differential negative mobility. At the outset of InP studies and predictions, it was not apparent which of these factors would be most dominant, but experimental results made clear that the noise figure of InP transferred electron amplifiers was far lower than equivalent GaAs devices [23, 24]. Noise figures as low at 7.5 dB were reported.

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[19] W. Fawcett and G. Hill, Elect. Lett. vol 11, 1975

[20] W. Fawcett, A.D. Boardman and S. Swain, J. Phys. Chem. Sol. vol 31, pp 1963-1990, 1970.

[21] C. Hammar and B. Vinter, Elect. Lett. 9, pp 9-10, 1973

[22] H. Kroemer, ECOM Report, ECOM-0016-F, Contract No. DAAB07-74-C-0016, 1974.

[23] S. Baskaran and P. Robson, Elect. Lett., 8, pp 137-8, 1972.

[24] P. W. Braddock and K.W. Gray, Elect. Lett., 9, 36-7, 1973.

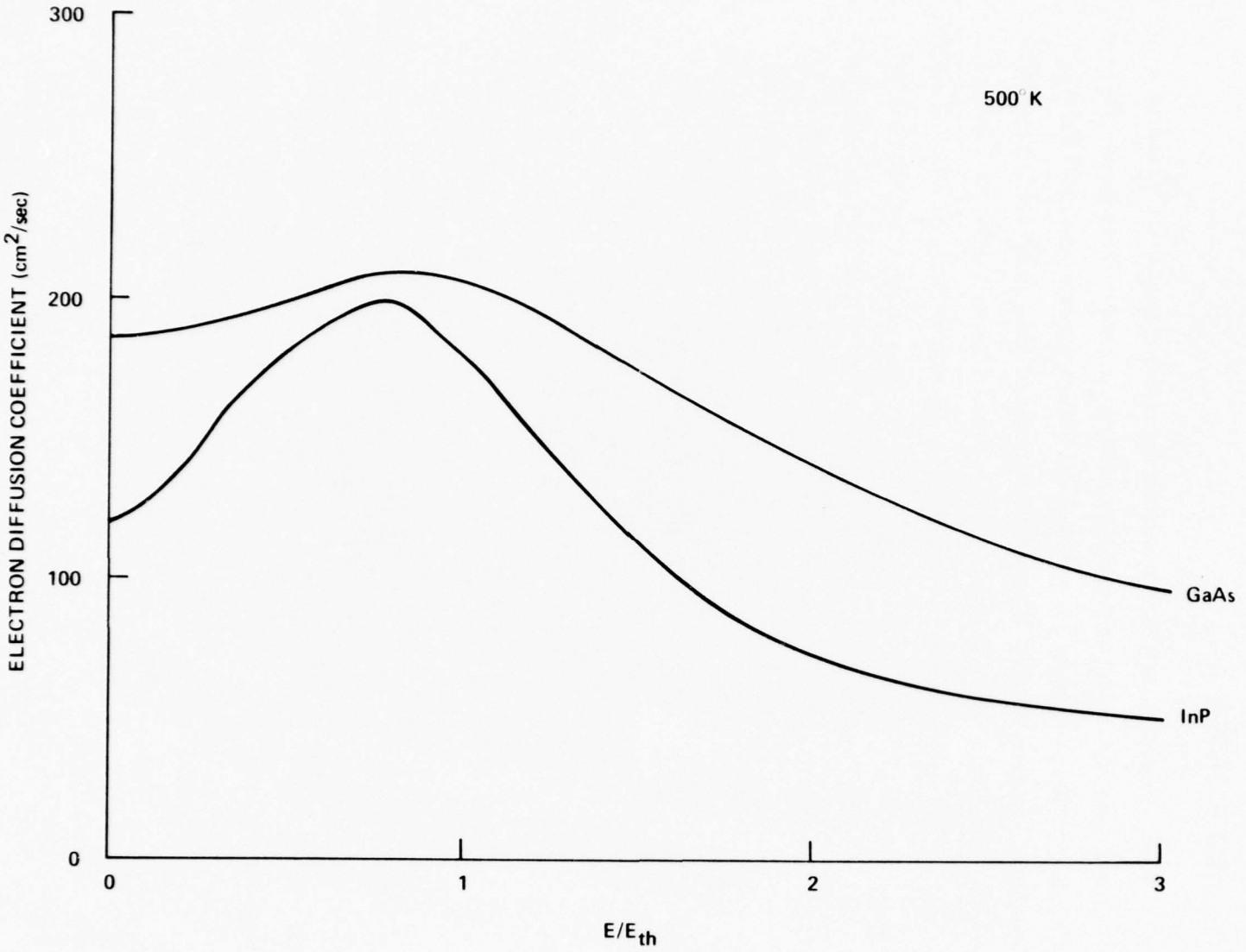


Figure 4.1. Comparison of Velocity-Field Characteristics for GaAs and InP as a Function of Temperature

At the outset of the present effort, it was evident that the successful realization of the device performance objectives was dependent upon establishing strict control over the material quality, carrier concentrations and length. Therefore, the majority of the effort spent in the first eight months of this one-year program was directed toward providing this level of capability as described in the preceding sections. This is particularly apparent from the strong predicted relationship between active region nL product and noise measure as shown in Figure 4.2 [5]. Well controlled doping profiles in the 1×10^{14} to 1×10^{15} cm^{-3} range are needed to approach theoretical limits of noise in the 26 to 40 GHz range for a conventional n^+-n-n^+ structure.

The strong predicted relationship between nL product and device noise measure can be understood by consideration of the dynamics of charge accumulation in the active region. An analytical solution of a simplified case has been discussed in depth by Robson [25]. In his approach, the noise measure is defined through an effective noise temperature

$$M = \frac{T_{eff}}{T_o} = \frac{\overline{Vn}^2}{4kT_o|R(\omega)|} \tag{2}$$

where $\overline{Vn}^2$ is the mean square open circuit noise voltage due to Johnson noise in the semiconductor and $|R(\omega)|$ is the magnitude of the device negative resistance. Both $\overline{Vn}^2$ and $R(\omega)$ are functions of the nL product since the amount of growth or accumulation occurring in a charge pulse while in transit is proportional to the fixed charge density and the transit time by a growth factor defined as

$$\zeta = \frac{Tn_o|\mu|e}{\epsilon} \quad . \tag{3}$$

This is, of course, also very dependent on the electric field through $|\mu|$ and v_o. The voltage across the device terminals which is a result of the charge in-transit is

[25]. P.N. Robson, The Radio and Electronic Engineer, 44 pp. 553-567 (1974)

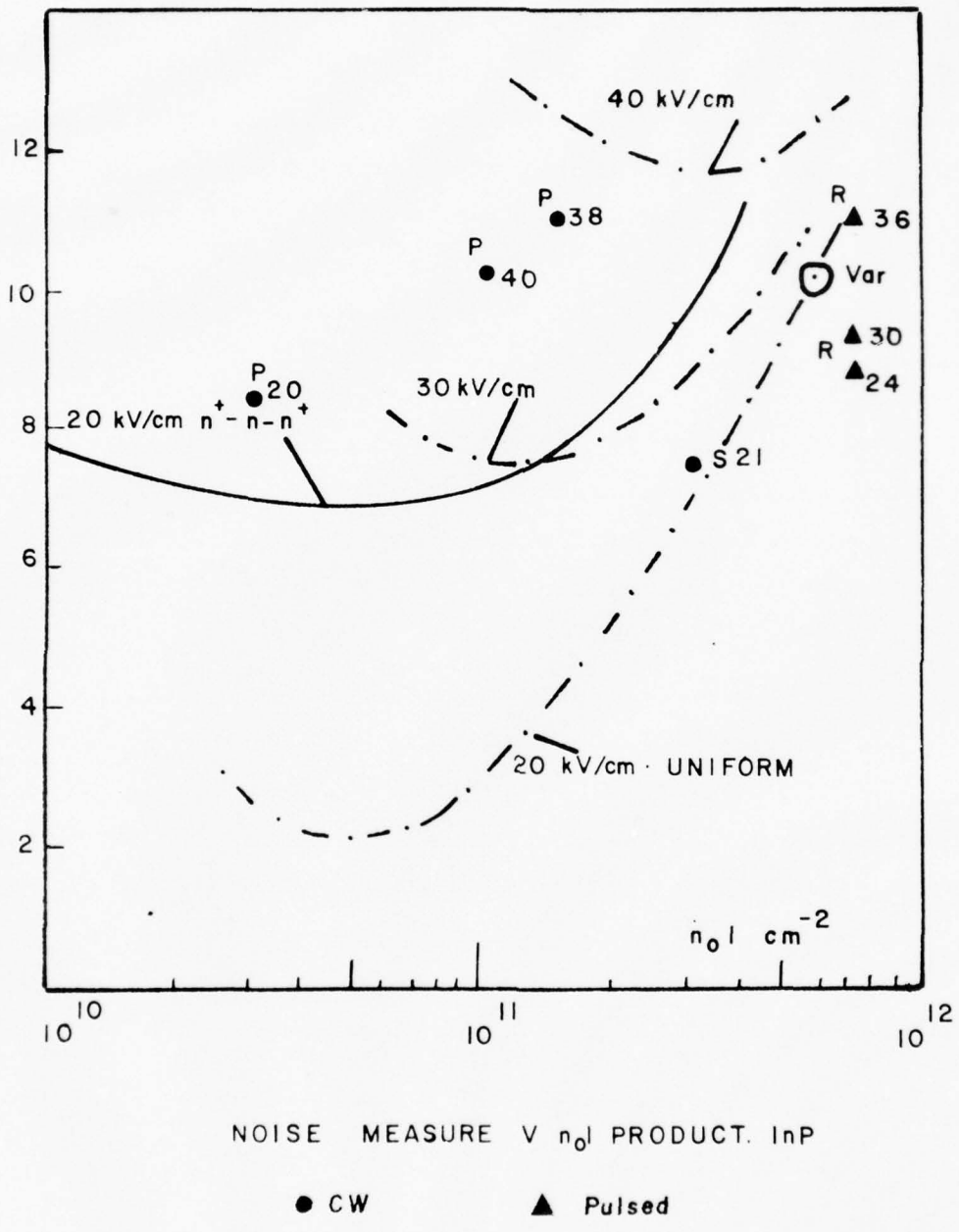


Figure 4.2. Variation of Minimum Noise Measure M with nl Product for Various Uniform Fields

related to a device impedance in the frequency domain by the Fourier transform. It is through this calculation that the impedance field method of Shockley et.al. [26] is related to the mean square noise voltage. The noise voltage decreases more rapidly with decrease in nL than the device negative resistance, hence the overall reduction in noise measure as the nL product is reduced.

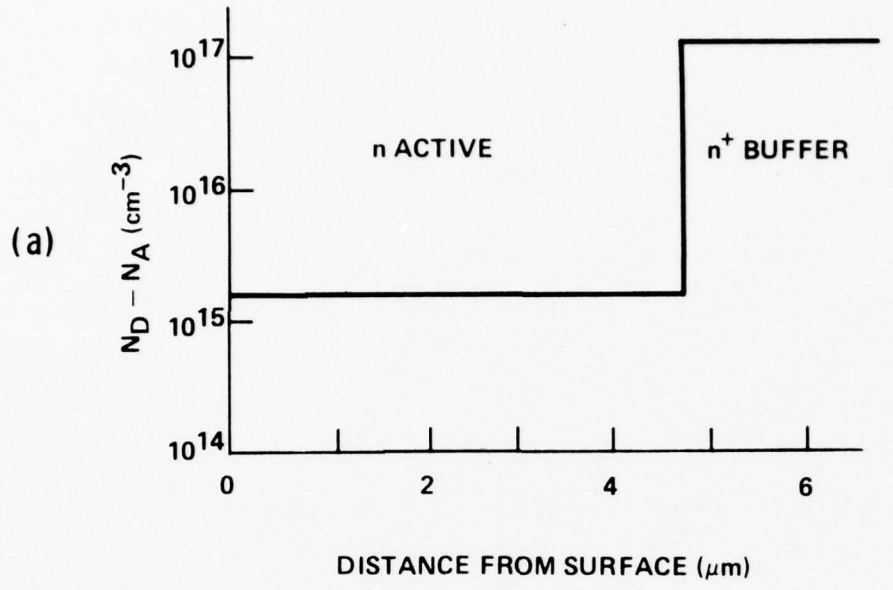
When the influence of hot electron diffusion is included in the analysis, the negative resistance decreases more rapidly at low nL products than $\overline{V}n^2$, hence the minimum noise measures shown in Figure 4.2. A more practical limit is reached sooner than this, however, due to the loss of negative resistance and consequent difficulty in achieving useful reflection gains over broad bandwidths. For further details on noise in TEA devices, the reader should consult one of Robson's papers [5, 25, 27].

In the present effort, two device structures have been evaluated as shown in Figure 4.3. Figure 4.3a shows an idealized doping profile for an n^+-n; buffer-active direct metal contact structure. This device type uses an alloyed Au-Ge/Ni ohmic contact directly on the epitaxial active layer as a cathode. The other type structure, shown in Figure 4.3b, consists of three sequentially grown layers in an n^+-n-n^+, buffer active contact sequence. In this case, the cathode is located at the n^+-n interface between the contact active or buffer active regions, depending upon the polarity of operation.

Comparisons of these two device types by rf performance, described in Section 5, have been indeterminate due to the much stronger dependence of performance on doping level and length. A summary of wafer properties grown for the 26.5 to 40 GHz amplifier application is given in Figure 4.4. Here, net carrier concentration is plotted against active layer length. Lines of constant nL product are drawn in for reference.

[26]. W. Shockley, J. Copeland and R. James, "Quantum Theory of Atom Molecules and Solid State", Academic Press, New York 1966.

[27]. J.E. Sitch and P.N. Robson, IEEE Trans. on Elect. Dev. ED-23, pp 1086-1094 (1976).



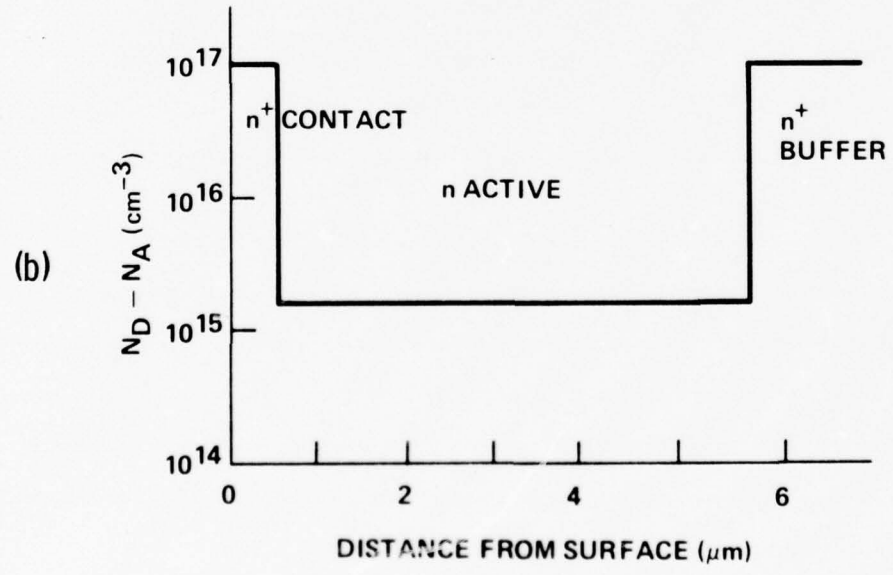


Figure 4.3. Idealized Doping Profiles of Two Ka-Band InP Structures
(a) Buffer Active n^+-n Direct Metal Contact
(b) Triple Layer n^+-n-n^+

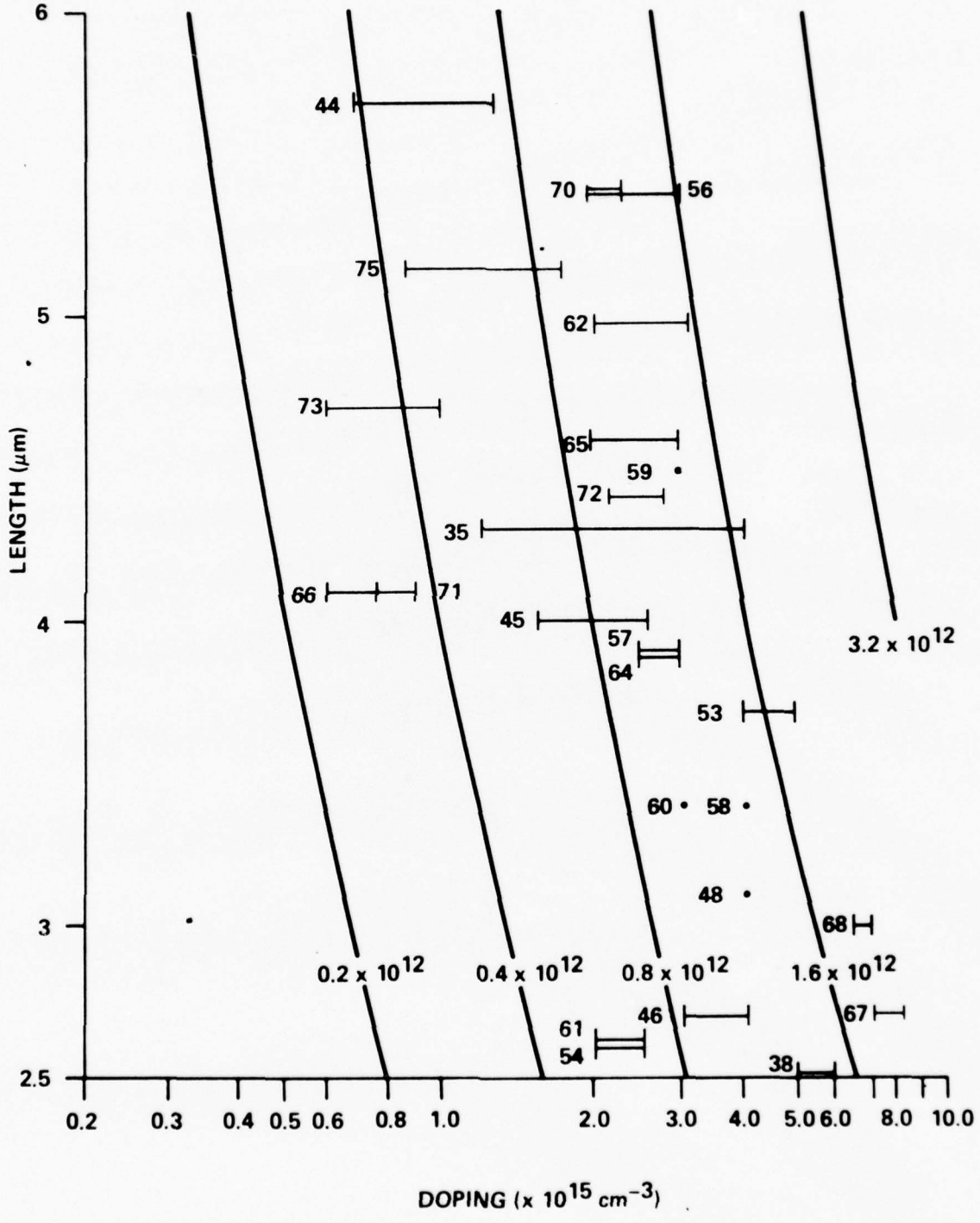


Figure 4.4. Wafer Doping and Length Summary

As a result of the wafers grown and evaluated for this program, certain general conclusions can be inferred from the rf testing described in Section 5. It was observed that reflection gain in the 26.5 to 40 GHz band could best be obtained using wafers with active layer lengths from 4.5 to 6 μm. The majority of the wafers evaluated had thicknesses at the lower end of this range and yielded peak performance in the 34-40 GHz range. Active layer lengths of 4.5 to 6 μm are longer than would be expected from an effective transit velocity of 1.3×10^7 cm/sec, but this probably is indicative of the more pronounced relaxation effects in InP which would contribute to a longer dead space at the cathode.

In general, higher reflection gain levels were experienced on wafers with doping levels of 2×10^{15} cm^{-3} or above. This is to be expected because of the higher nL product. Above 3×10^{15} cm^{-3}, it was difficult to stabilize the device against out-of-band oscillation. The higher gain levels were obtained at the expense of noise figure. Best low noise performance was observed on wafers with active layer doping levels less than $1 \times 10^{15} cm^{-3}$. Gain bandwidth product was reduced, however, so reasonable gain levels could only be obtained in 5 GHz or small bandwidth amplifiers. A more detailed discussion of specific wafer performance can be found in Section 5.3.

It has also been noticed that operation in both polarities (heat sink negative or normal polarity and heat sink positive or reverse polarity) has been possible, in many cases, with both grown n^+ and direct metal contacts. This is contrary to experience on GaAs TEA diodes. Also in many cases, superior reflection gain was obtained in the reverse direction, possibly due to the generally higher operating voltages permitted by the improved heat conduction path from anode to heat sink. Low nL product devices had poorer gain in the reverse polarity.

4.2 CONTACTS

The region about threshold is to be avoided in a low noise amplifier design because of the peak in the electron diffusion constant and consequent higher noise generation as shown by equation (1). Also, high electric fields are not desirable because of the small μ associated with them through the GaAs or InP velocity field characteristic. In InP, an electric field of 15-20 kV/cm is optimum for minimum noise generation.

Realization of this optimum electric field is not possible with the n^+-n-n^+ structures shown in Figure 4.3b. Solutions of the Poisson and continuity equations yield very non-uniform electric field distributions over a wide range of active layer doping and length combinations. Low electric field near the cathode and high electric field at the anode are always obtained. Since a uniform electric field profile is necessary to operate in the minimum noise generation region, departures from the flat doping profile or ohmic contact of Figure 4.3 are needed.

Even though noise measure is reduced in n^+-n-n^+ structures by utilization of a low nL product, theoretical limitations due to the injected space charge limited currents from the n^+ cathode prevent realization of the ultimate capability of InP. Also, gain-bandwidth product is severely limited for low nL devices because of the small negative real part and the consequent difficulty of realizing broadband matching circuits for low impedance, high Q devices.

A logical way to overcome these limitations is presented by the cathode notch contact approach as described in Figure 4.5. This cathode notch zone of lower donor density provides an acceleration region for electrons, driving them above threshold in a narrow spatial zone. In addition, if the notch width and length is properly selected, the injected space charge at the downstream end of the notch can be forced to equal the fixed donor density, hence achieving space charge neutrality and flat or uniform electric field in the active region by

$$\frac{dE}{dX} = \frac{q}{\epsilon} (n - N_D). \tag{4}$$

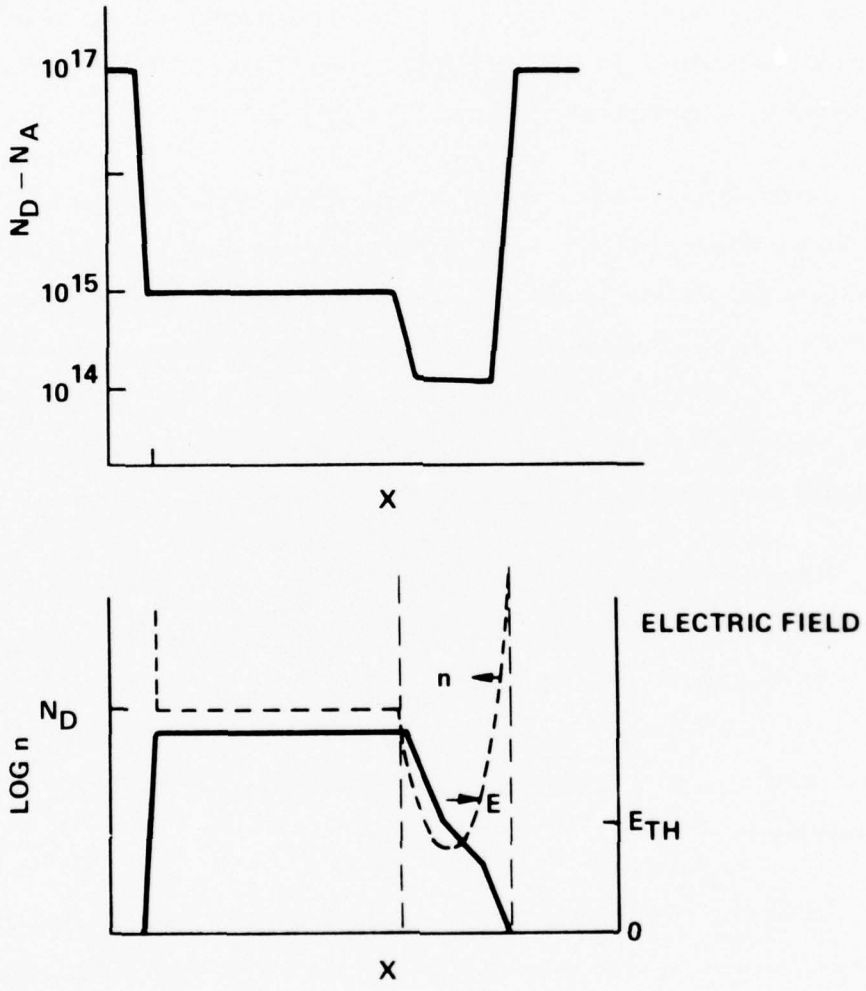


Figure 4.5. Proposed Cathode Notch Doping Profile

Both operating field and current density can be controlled by the notch doping and length. This structure reduces noise measure due to generation at low fields and loss of $|\mu|$ at high fields and should allow use of more highly doped active regions to maintain gain bandwidth product. Referring back to Figure 4.5, a net reduction in noise measure of several dB is predicted for uniform electric field InP diodes [5]. Also, the electric field distribution should not be as critically dependent on operating voltage, which will help reduce AM noise due to upconverted power supply variations.

Preliminary calculations have been completed for the design of cathode notch amplifier devices in the 26.5 to 40 GHz range. This is accomplished by a numerical solution of equation 4 using a curve-fit approximation to Fawcett and Herbert's velocity-field characteristic at 500° K and the drift current density

$$J = nq\ v\ (\epsilon). \tag{5}$$

Effects due to diffusion are negligible. These equations are solved assuming that for a given electric field, the space charge equals the active layer fixed charge at the active-notch boundary. A simple linear extrapolation through the notch region is performed at small enough increments in space to permit accurate convergence. Thus, for a known active region doping, electric field and notch doping, the correct notch length can be obtained.

The results for one typical case are summarized in Figure 4.6. In the case of InP, the cathode notch region must be deeper and/or wider than that required for GaAs devices. Maximum width is limited to 1.5 μm or less to provide significant acceleration zone benefits and to minimize voltage drop across the notch. In competition with this requirement, the nL product of the active layer must be low to achieve the minimum in noise measure. This requires that the doping of the notch be very low (or even slightly P-type) to provide the ultimate noise measures in InP. This will require significant improvements in InP epitaxial growth technology.

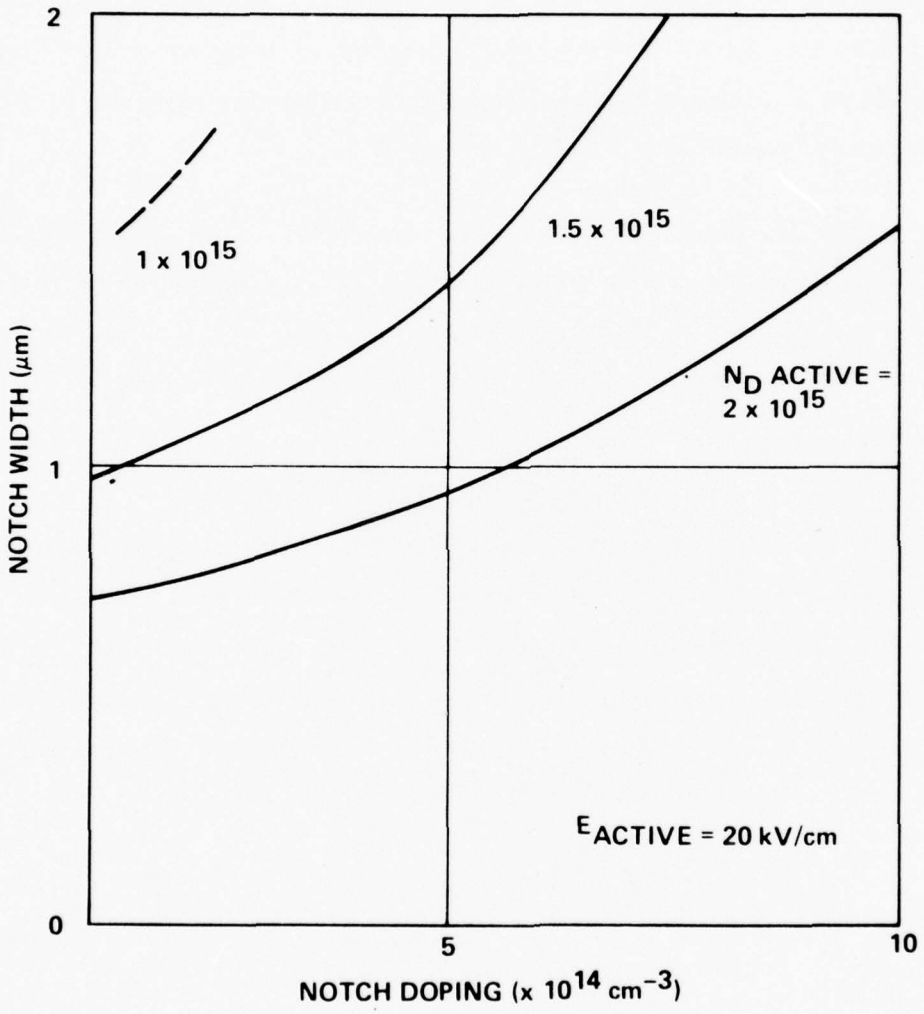


Figure 4.6. Calculation of Notch Width and Doping for Selected Active Region Dopings of an InP Cathode Notch Device

After weighing the above factors, a theoretical Ka-band device design has been determined. The active layer is to be 4.5 μm in length, slightly less than the 4.5 - 6 μm length as determined from rf measurements of flat doping profile devices, but consistent with trends in GaAs flat profile and cathode notch device performance. Active layer doping should be in the range of 1 to 1.5 x 10^{15} cm^{-3}. Notch doping and length can be determined from the graph presented in Figure 4.6. In this figure, notch doping and width are compared for optimum noise reduction at three active layer doping densities.

4.3 FABRICATION METHODS

4.3.1 Ultrasonic Bonding

Two processes were employed for fabrication of InP devices. The first process, scribe and cleave ultrasonic bonding, was used on all wafers evaluated for this program. The success of this approach depends on such variables as the surface quality of the epitaxial layer, the precise bonding conditions utilized (pressure, temperature, ultrasonic amplitude), and the effectiveness of the cleanup etch in removing scribe and bonding damage from the chip surface. The device operating current must also be controlled by the in-package etchant, a separate problem which will be further discussed. The majority of the rf results reported in Section 5 were obtained from devices fabricated in this manner.

4.3.2 Integral Heat Sink

In order to control the thermal resistance more reproducibly and to simplify the bonding process, a gold-plated integral heat sink process (IHS) similar to that used for GaAs Gunn devices was desired. This type of approach has several distinct advantages over the scribe and cleave approach. Wafers are not reduced to chips by a mechanical process; a carefully controlled etching process is employed. Since the plated heat sink is in close contact with the epitaxial layer, small surface

irregularities do not destroy the thermal contact. Thus, the thermal resistance of these devices, while not always lower than the ideal TC or ultrasonically bonded device, consistently approaches the theoretical minimum for the particular device area and geometry.

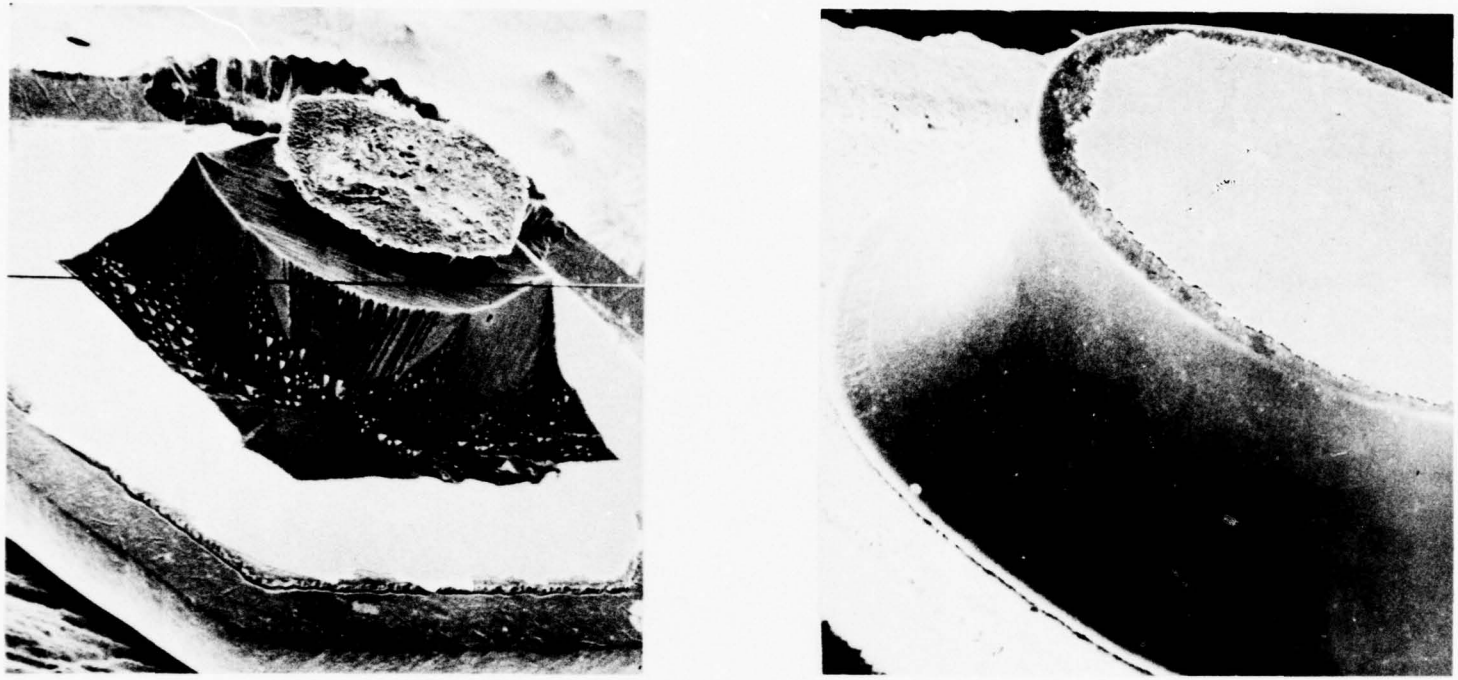
The adaptation of GaAs IHS processes to mm-wave InP wafers was initially impeded by lack of a suitable polishing (isotropic) etchant which does not rapidly attack gold. Due to the formation of very stable surface oxides, oxidizing etchants are prevented from attacking InP surfaces. At the present time, only bromine-based etchants have isotropically etched InP with successful results. HCL has highly anisotropic etch rates which result in severe surface faceting, as shown in Figure 4.7a. The aqueous Br HBr etchants have been found to be moderately isotropic, have reduced attack rates on gold, and permit use of positive or negative photo-resists. An etchant similar to that reported by Brookbanks et al [28] was used to etch the mesas shown in Figure 4.7b.

Several plated gold IHS fabrication sequences have been evaluated and are still in development. The first two of these processes are outlined in the flow charts of Figure 4.8 and 4.9.

The first process utilizes a pre-thinned wafer (50 microns thick) with alloyed Au-Ge/Ni contacts on both sides. After heat-sink plating, contact pads are defined and mesas are etched until the heat sink is reached. While this process works exceedingly well for larger diameter mesas (> 4 mils), the small-device areas required for cw Ka-band InP Gunn diodes were impossible to etch on 50 micron thick wafers without excessive undercutting. While thinner wafers have been processed successfully, the loss in yield due to breakage or accidental cleaving would, on the average, be excessive.

For this reason, a second process was conceived in which the heat sinks could be plated prior to wafer thinning to provide mechanical support. An ohmic contact

[28] D.M. Brookbanks, I. Griffith and P.M. White, Metal-Semiconductor Contacts, Conf. Series 22, Inst. Phys., London, 1974.



(a) (b)

Figure 4.7. (a) Severe Faceting Effects of HCl Anisotropic Etchant
(b) Moderately Isotropic Mesa Produced by Aqueous Br-HBr Etchant

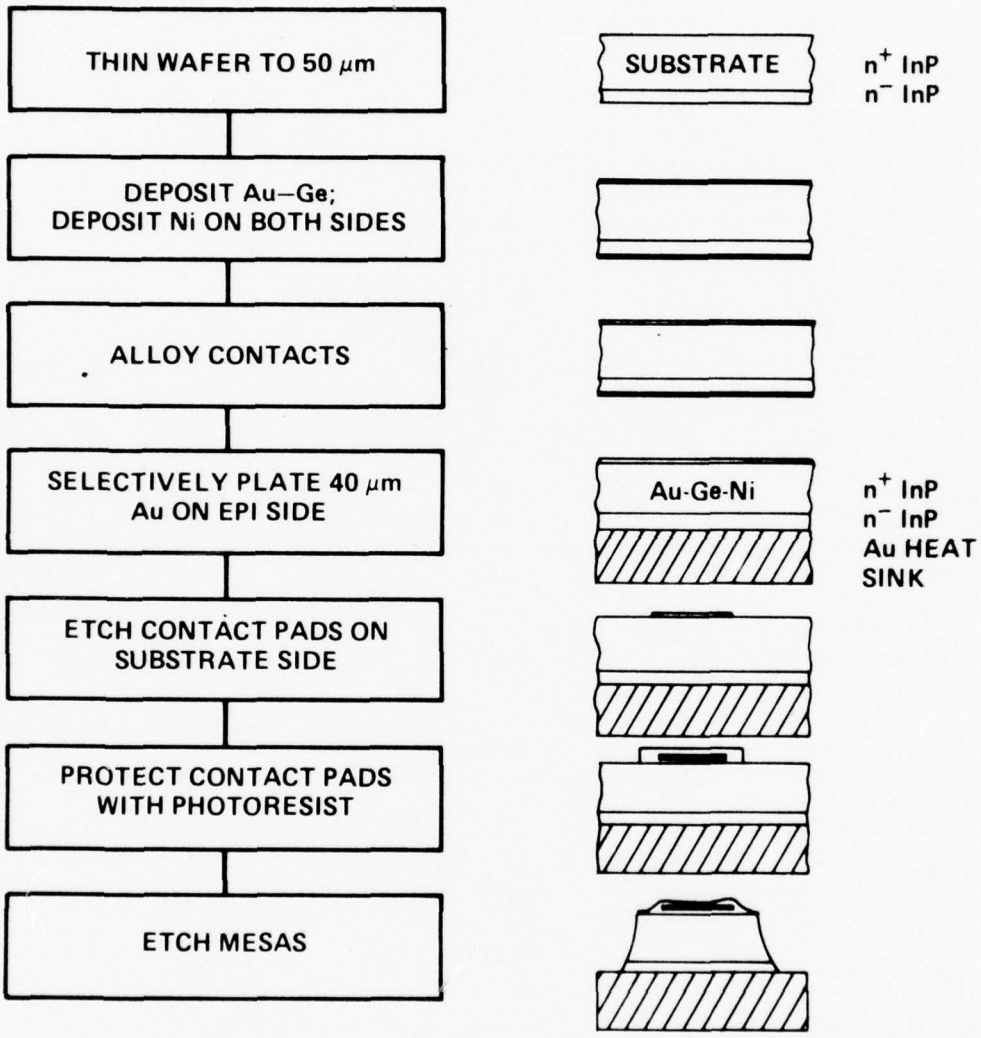


Figure 4.8. Flow Diagram Showing Fabrication Sequence for Integral Heat Sink Process No. 1

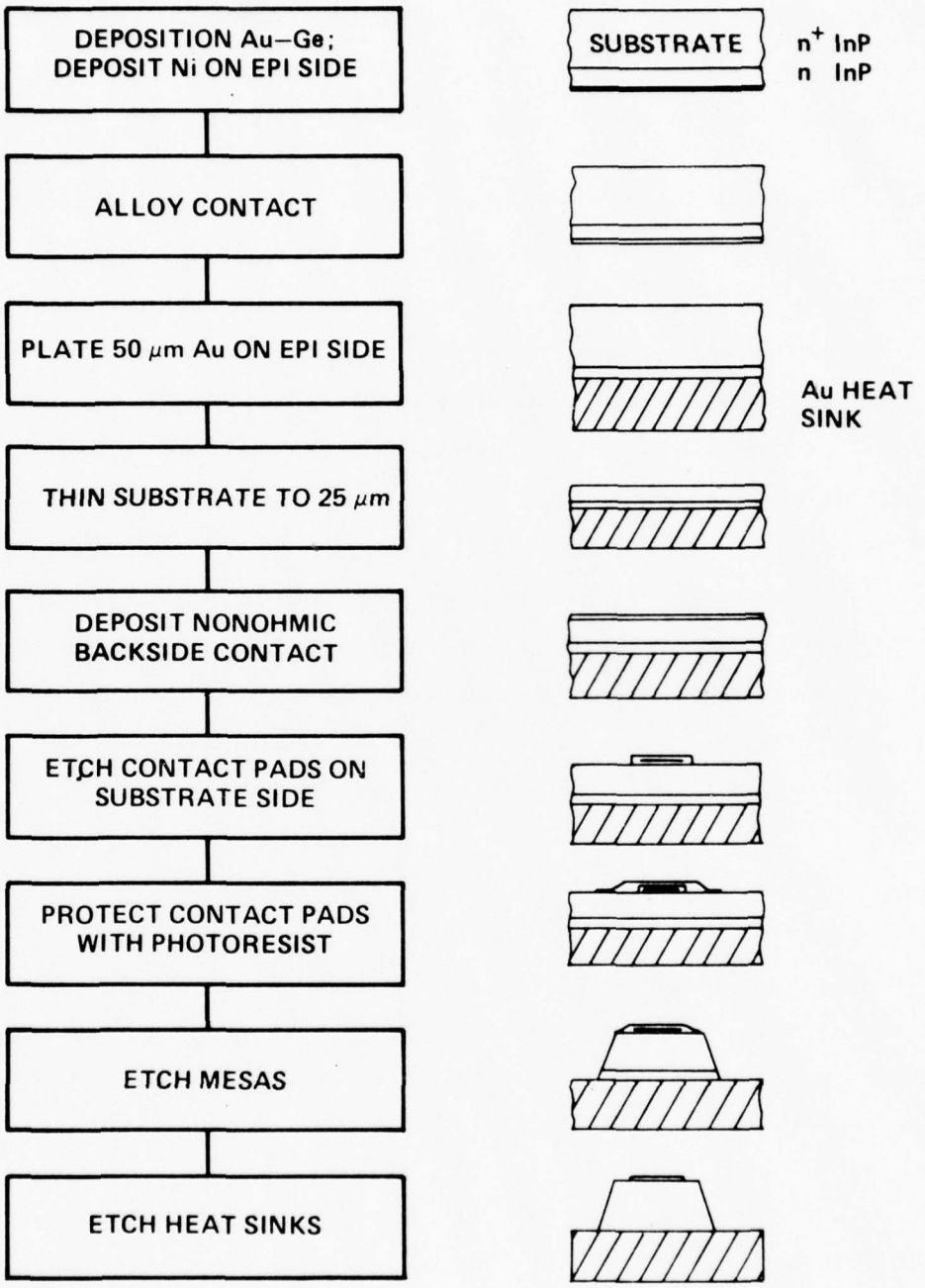


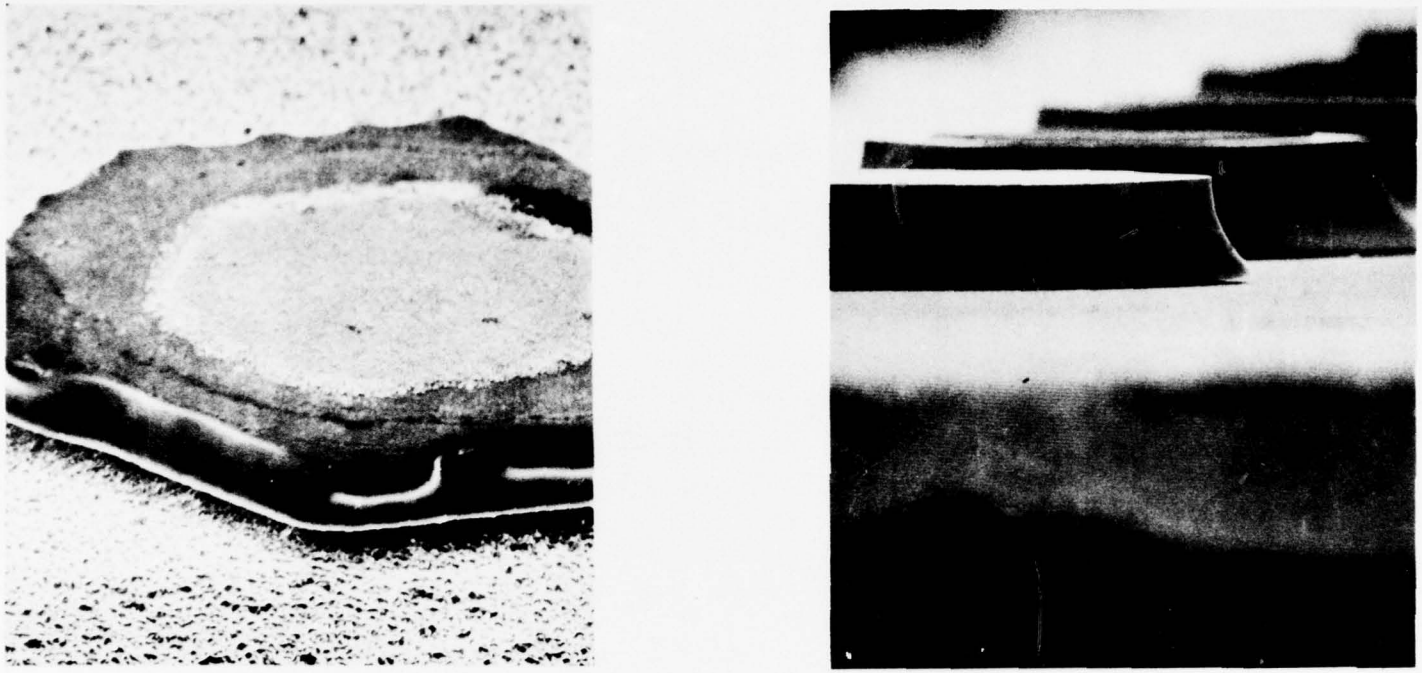
Figure 4.9. Flow Diagram Showing Fabrication Sequence for Integral Heat Sink Process No. 2

is deposited and alloyed on the epi side, followed by 40-50 microns of plated gold. The substrate was then reduced in thickness to 25 microns, using Br-methanol on a polishing pad. A non-ohmic (forward-biased Schottky barrier) contact of nickel gold was deposited on the substrate and the mesa etch followed.

This second approach was used on wafer EE46. Yield of good chips was limited by the non-uniformity of polishing and the plating thickness non-uniformity. Polishing flatness was significantly improved by the use of polishing stops which prevent excessive mechanical or chemical polishing and minimize rounding of wafer edges. Even with the improvements in polishing, wafer thickness variations from 10 to 30 μm were not uncommon, largely due to non-uniformity of the plated heat sink. To minimize this problem, an approach was evaluated which utilizes a conductive plating carrier so that edge effects on small wafers are reduced significantly. This approach also has the advantage of normalizing plating current and permitting several wafers to be plated at the same time. This technique has reduced the average wafer thickness variation after polishing to a more tolerable 10 to 20 μm range; however, further improvements are needed to insure mesa diameter uniformity across a typical 1 cm^2 wafer section.

At this stage, detailed SEM analysis of etched InP mesas on the plated gold heat sink revealed an additional problem which is still under investigation. Figure 4.10a shows an SEM photograph of a chip revealing extensive undercut of the InP mesa and gold contact metallization by the etchant. This was attributed to the reactivity of the Br etchant with gold metallization. This undercut totally destroys the thermal contact between device and heat sink.

To limit the attack of gold, an additional approach was evaluated which interposed a platinum etch barrier layer between the Au-Ge/Ni contact metallization and the plating. This was successful in reducing the extent of etchback into the heat sink as shown in Figure 4.10b; however, it can be seen that undercut of the InP still occurred, even in relatively brief exposure intervals.



(a) (b)

Figure 4.10. (a) InP Mesa Etched on Gold Plated Heat Sink. Diameter is Approximately 100 μ m.

(b) InP Mesa Etched on Pt Etch Barrier

It seems evident, therefore, that the very rapid undercut observed is primarily occurring in the InP itself and not in the metallization. This could be caused either by interfacial strain or by electrochemically accelerated etch processes at the interface, possibly due to hole injection into the lightly doped n - InP. Further investigations into this problem will be made.

In any of the integral heat sink processes in which the wafer is thinned after the heat sink is plated, separation of devices must take place as the final process step. To accomplish this, a photoresist masking step has been followed by a spray etching technique which etches the gold plating between mesas. This approach has been evaluated and has been found to produce very well defined, near-vertical edges on the heat sinks.

4.3.3 In-Package Etching

It is desirable to use a clean-up or current adjustment etch after devices are bonded in the ceramic packages to remove any surface contamination and select the threshold current. Due to the problems outlined above regarding gold attack by Br-based etchants, this has not been accomplished. Gold-plated package parts are attacked too rapidly to permit utilization of these etchants. HCl has been used; however, its preferential etch rates lead to very unsatisfactory mesa geometrics. This emphasizes the need for good control of mesa diameter in the chip fabrication process, so that only very brief in-package etches are necessary.

4.4 THERMAL RESISTANCE

In order to evaluate the effectiveness of the device fabrication and bonding processes, device thermal resistance measurements were employed. These measurements utilized the temperature dependence of the low field mobility to determine actual device active layer temperatures. To accomplish this, devices are calibrated by measuring bias voltage for a constant bias current (10 mA) at three ambient temperatures. Once the diode temperature - voltage characteristic is established, device active layer temperatures are measured while dc biased under non-oscillating

conditions by pulsing down to the calibration current level. This pulse down employs a very low duty cycle, short pulse to prevent alteration of the device temperature. The resulting low field bias voltage is related to the calibration data and thermal resistance determined by:

$$\Theta_T = \frac{T_{device} - T_{heat\ sink}}{P_{in}}$$

where P_{in} is the dc average heating bias applied to the device under test.

Ideal device thermal resistances were calculated for each device knowing the active layer doping and length and the operating current. Device areas were inferred from the conduction current assuming an effective transit velocity of 1.3×10^7 cm/sec. The theoretical values were calculated using the following equation:

$$\Theta_T = \frac{l_{nn+}}{k_{InP}\,\pi r^2} + \frac{1}{4\,k_{cu}\,r} + \Theta_P$$

where:

k_{InP} = thermal conductivity of InP at 200° C
= 0.35 w/cm-deg.

k_{cu} = thermal conductivity of copper
= 3.9 W/cm-deg.

$l_{nn}+$ = length of epitaxial InP between anode and heat sink

Θ_P = package and bonding contribution
$\cong 3°$ C/W

r = radius of device

$$r = \sqrt{\frac{I_{op}}{nq\,v_{eff}\,\pi}} = 1.53 \times 10^{11} \frac{I_{op}}{n}$$

n = device active layer carrier concentration

Measurements were made on two instruments. One of these, a manual instrument, used an oscilloscope for pulse down voltage measurements. This yielded the most reliable results. The second instrument, a commercially manufactured automatic unit, utilizes sampling techniques to determine average voltages and calculates thermal resistance using the empirical temperature calibration factor. Unfortunately, this second technique was not reliable, possibly due to low frequency bias oscillations.

Measured results are presented Table 4.1. Doping levels and theoretical thermal resistances are compared to those measured by both instruments. As would be expected, thermal resistance is inversely proportional to doping. That is, the lower doped wafers require larger areas for the same operating current and therefore have lower thermal resistance.

TABLE 4.1

THERMAL RESISTANCE MEASUREMENTS

WAFER	DOPING $\times 10^{15}$	AVERAGE THERMAL RESISTANCES (° C/W) THEORETICAL	MANUAL	AUTO
67	7-8	52	94	30
71	.75-.9	19	38	23
72	2.1-2.5	28	36	25
73	.6-1.0	27	29	---

5. DEVICE EVALUATION

5.1 DEVICE PARAMETERS INVESTIGATED

In an effort to provide feedback of information for the material growth and device design aspects of the program, a thorough rf evaluation of all wafers with promising dc characteristics was carried out through measurement of several device parameters. Gain was measured on a Ka-band reflectometer setup in a variety of test cavities which cover the entire 26-40 GHz frequency range. Circuit parameters were optimized to increase gain or stabilize oscillations, depending upon the level of negative resistance the device exhibited. This information, together with knowledge of the device doping level, allowed us to generally rate the performance of the devices. The optimum frequency range was practically determined by which circuit-device combination yielded the highest negative resistance level.

If the wafer showed good promise in terms of device reliability and had reasonable gain levels, it was evaluated for noise figure and noise measure, using a circulator to couple the signal into and out of the amplifier. If the wafer had good noise figures as well, other evaluations such as impedance and compression characteristic measurements were then performed.

5.1.1 Test Circuit Description

Analysis of a wafer was performed in lower and upper half band amplifier circuits similar to those used for GaAs Gunn amplifiers on previous programs. This circuit consists of a coax line of approximately 65 Ω terminated on one end by the Gunn device and on the other by a multisection low-pass filter for dc bias insertion. A portion of the outer coax conductor is cut away and forms a reduced-height section of waveguide. This feature provides both coax-to-waveguide transformation and impedance transformation to the full-height output waveguide. Figure 5.1 presents a cross-sectional view of this amplifier circuit. The circuit is frequency scaled and otherwise modified to provide operation over the 26.5 to 33, 29 to 37 and 33 to 40 GHz segments of the band. Circuit optimization for individual devices is

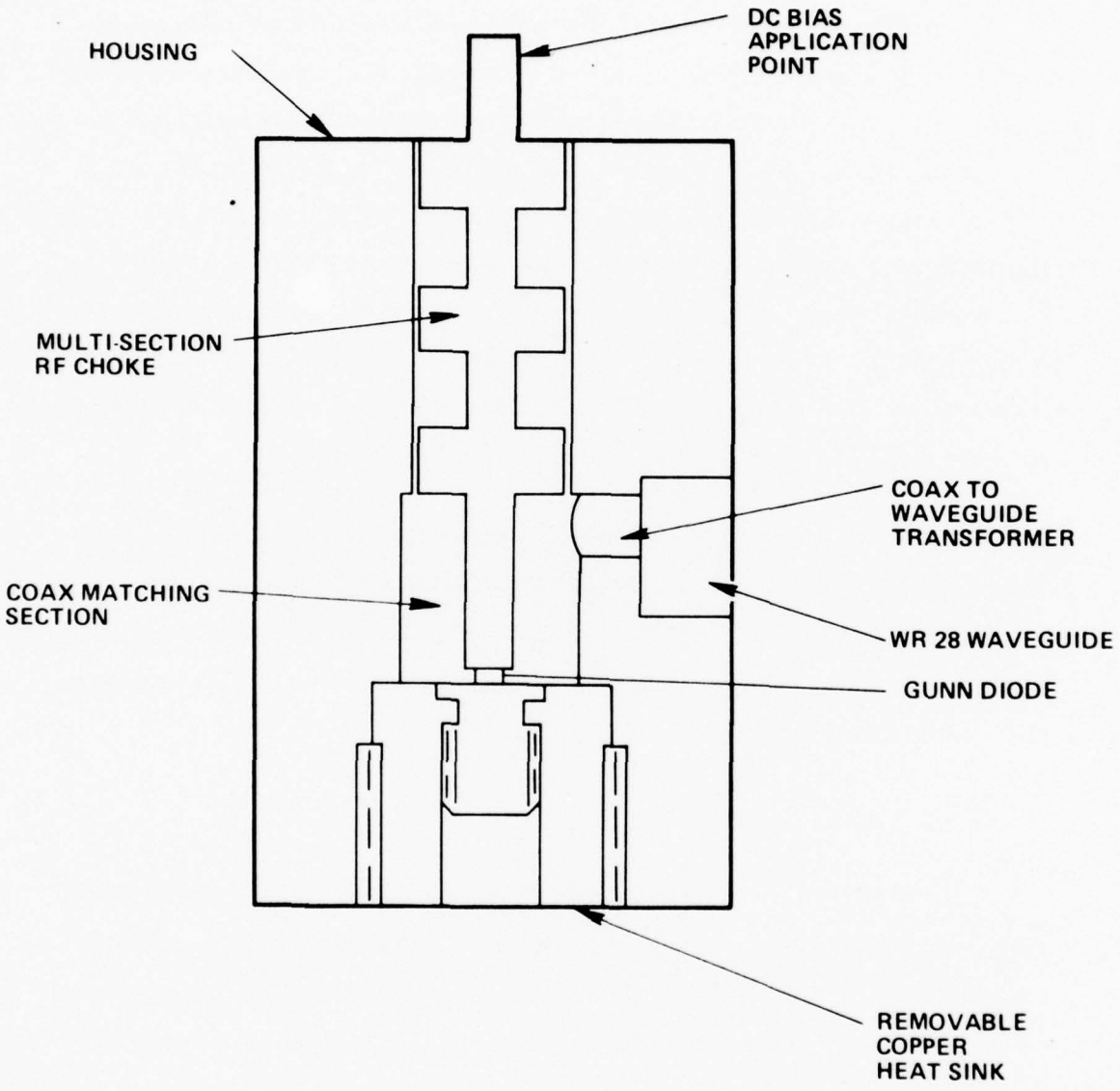


Figure 5.1. Cross-sectional View of Coaxial-Waveguide Hybrid Amplifier Circuit

accomplished by varying the center conductor length and/or diameter; coupling can be varied by external means, such as a slide screw tuner or tuning block. The latter is usually required only with very low-gain, low-doped devices and results in a high-gain, narrow-band amplifier configuration which enables noise figure analysis to be performed.

Wide band (>4 GHz) gain levels are typically in the 4 to 12 dB range with the upper limit being set by stability considerations. Gain levels higher than this are impractical near frequency band limits of waveguide components and when using circulators to provide nonreciprocal performance, because mismatches presented to the amplifier can lead to wide gain variations or instabilities.

5.1.2 Parameter Measurements

This section briefly summarizes how the various device rf parameters were measured and what types of equipment were used.

For gain/bandwidth measurements, the amplifier circuit was mounted directly on the input port of a high directivity (40 dB) 10 dB coupler. A detector was placed on the coupled arm with a variable attenuator in series to improve the match. Swept and leveled power was applied to the coupler's output port. This simple and easily calibrated reflection test setup gives very repeatable results, as displayed on either a frequency response network analyzer or an X-Y recorder. It also provides very simple compression tests when uniformly varying the input power and the attenuation just in front of the detector.

Noise figures were measured in one basic configuration, but equipment types and procedures were varied to give the most realistic picture possible. The circuit/device combination was tuned on a circulator with optimum frequency performance matching that of the amplifier. Gain levels were recorded for device noise measurement calculations. A noise tube was then substituted for the input signal and a variable attenuator was placed between the amplifier output and the low noise mixer signal input port. This commercially available mixer had very low noise performance

(7.2 to 9.0 dB measured across the entire Ka-frequency band) and was operated with approximately 2 mW L.O. drive. Noise figures were measured using a 30 MHz I. F. frequency, and using either the automatic mode (with two different manufacturers' noise figure meters) or manually, using the Y-factor method.

5.1.3 Impedance Measurements

Devices from several wafers were characterized in the half band amplifier circuits using slotted line techniques to measure the active reflection coefficient. In this procedure, the circuit Z-matrix is measured using three offset shorts in place of the packaged device in the amplifier circuit; the circuit is characterized to the TEM reference plane at the top of the diode package. Phase information is obtained using slotted line measurements. The active device is then substituted for the offset short and biased to the desired stable operating point. Slotted line measurements are again made to determine SWR and phase information. This information is then reduced to R and X impedance data, using computer programs. The data are then plotted on Smith charts and bandwidths, negative resistance levels, device Q, etc. can be easily determined.

5.2 COMPREHENSIVE RESULTS SUMMARY

5.2.1 Material Properties and RF Performance

During the course of the twelve month effort, over 30 wafers were grown and a high percentage evaluated for use as Ka-band amplifiers. This section presents a complete summary of all wafers grown and tested. Better performing wafers are treated individually in a later section.

Table 5.1 presents a summary of material properties of wafers grown for the amplifier program. Two-thirds of the wafers grown were evaluated as amplifiers. Reasons for not evaluating a wafer include high resistivity material, poor metal adhesion or problems with dc characteristics. Figure 4.4 in Section 4.1 gives a graphical display of $n_o xl$ product values for the wafers grown. As would be expected, stability problems were encountered with devices having lengths shorter

TABLE 5.1

MATERIAL PROPERTIES OF
InP WAFERS SELECTED FOR AMPLIFIER
EVALUATION IN THE 26-40 GHz RANGE

WF /RUN	M	SC	IHS	RF	nx10^{15}	ACTIVE LAYER LENGTH (μm)	TYPE
EE33/IP3-2	X	X		X	2.5 - 2.8		DM
EE35/SSW 11-9	X	X		X	4 - 1.2	4.3	DM
EE37/SSW 11-10	X	X		X	8 - 7	4.9	DM
EE38/SSW 12-5	X	X		X	5 - 6	2.5	DM
EE39/SSW 12-5	X	X		X	5.5	2.5	DM
EE44/Sr InP 2-4	X	X		X	1.3 - 0.5	5.7	DM
EE45/SR InP 2-5	X	X		X	2.6 - 1.6	4.0	DM
EE46/SSW 20-2	X	X	X	X	3 - 4	2.7	DM
EE48/SSW 20-5	X	X	X	X	4	3.1	G
EE53/SSW 20-10	X	X		X	4 - 5	3.7	G
EE54/SSW 21-2	X	X	X		2 - 2.5	2.6	G
EE55/SSW 21-3	X	X	X	X	1.4 - 1.5	1.9	G
EE56/SSW 21-4	X	X	X	X	2 - 3	5.4	G
EE57/SSW 21-5	X	X			3 - 2.5	3.9	G
EE58/SSW 21-6	X	X			4	3.4	G
EE59/SSW 21-7	X	X		X	3	4.5	G
EE60/SSW 21-8	X	X			3	3.4	G
EE61/SSW 21-2T	X	X			2 - 2.5	2.64	DM
EE62/SSW 21-4T	X	X		X	2	5.4	DM
EE64/SSW 22-2T	X	X			2.5 - 3	3.9	DM
EE65/SSW 22-4	X	X		X	2 - 3	4.6	G
EE66/SSW 22-5	X	X		X	0.75 - 0.6	4.1	G
EE68/SSW 22-8	X	X			6.5 - 7	3	G
EE70/SSW 21-4	X	X		X	2 - 2.3	5.4	G
EE71/SSW 22-5	X	X		X	.75 - .9	4.1	G
EE73/SSW 27-3	X	X		X	.6 - 1	4.7	G
EE74/SR 10-7	X	X			.4 - .8	6.64	G
EE75/SR 10-8	X	X			.5 - 1	5.2	G
EE76/SR 10-9	X	X			.7 - 1	8.3	G
EE77/SR 10-9	X	X	X		.7 - 1	8.3	G

M = metallization
SC = scribe and cleave
IHS = integral heat sink
RF = RF evaluation
DM = direct metal contact
G = grown n^+ contact

than 3μm or dopings higher than 3×10^{15} cm^{-3} when evaluated in Ka-band amplifier circuits. Although this will be outlined in greater detail in a later section, optimum performance was obtained in Ka-band with devices having the following characteristics:

Frequency Range	n_o	l
Upper 1/2 band	0.8×10^{15} cm^{-3}	4.2 μm
Center band	0.75×10^{15} cm^{-3}	4.4 μm
Lower 1/2 band	0.7×10^{15} cm^{-3}	4.7 μm

Looking only at those devices giving stable amplification in Ka-band, we can generate Table 5.2 which lists several measured and calculated parameters. The gain levels are those seen over the corresponding bandwidths. The gain-bandwidth product is calculated by taking the square root of the average voltage gain ratio and multiplying it by the bandwidth in GHz. Noise figures are device noise figures. Losses attributable to circulator and circuit as well as receiver noise contributions have been subtracted.

5.2.2 Gain Measurements at Frequencies greater than 40 GHz

RF evaluation was performed on devices from several wafers in the 40 to 60 GHz frequency range at NELC's San Diego facility. The amplifier circuit used on the 40 to 60 GHz reflectometer was in the 38 GHz circuit and useful gain extended to approximately 47 GHz. Results from some of the devices are presented in Figures 5.2 and 5.3. In Figure 5.2, gains for two devices from wafer EE35 are presented. This device has an active layer length of 4.3 μm and an active layer doping of $4\text{-}1.2 \times 10^{15}$ cm^{-3} for an effective nxl product of $0.5 - 1.7 \times 10^{12}$. Other devices measured in the same circuit and frequency range are shown in Figure 5.3. Table 5.3 summarizes performance and device parameters in this frequency range.

TABLE 5.2

RF PERFORMANCE SUMMARY FOR BETTER AMPLIFIER WAFERS

Wafer (EE No.)	Gain (dB)	Frequency Range (GHz)	Gain x BW ($\sqrt{G_V}$ x GHz)	Noise Figure (dB)	Noise Measure (dB)
33	5 - 10	28 - 38	15	14 - 17	16 - 19
35	4 - 6	38 - 40	2.7	high	x
44	2	30 - 38	1.0	11 - 12	12 - 14
56	4	34 - 39	4.2	-	-
57	8 - 12	38 - 40	3.6	high	x
59	4 - 6	35 - 40	12	15 - 16	17 - 19
66	3	37 - 39	6.7	9 - 11	14 - 16
70	5 - 10	35 - 40	7	13 - 16	15 - 18
71	4 - 6	34 - 39	5.7	9-11	11 - 13
73	1 - 2	30 - 36	4.5	14 - 15	15 - 17

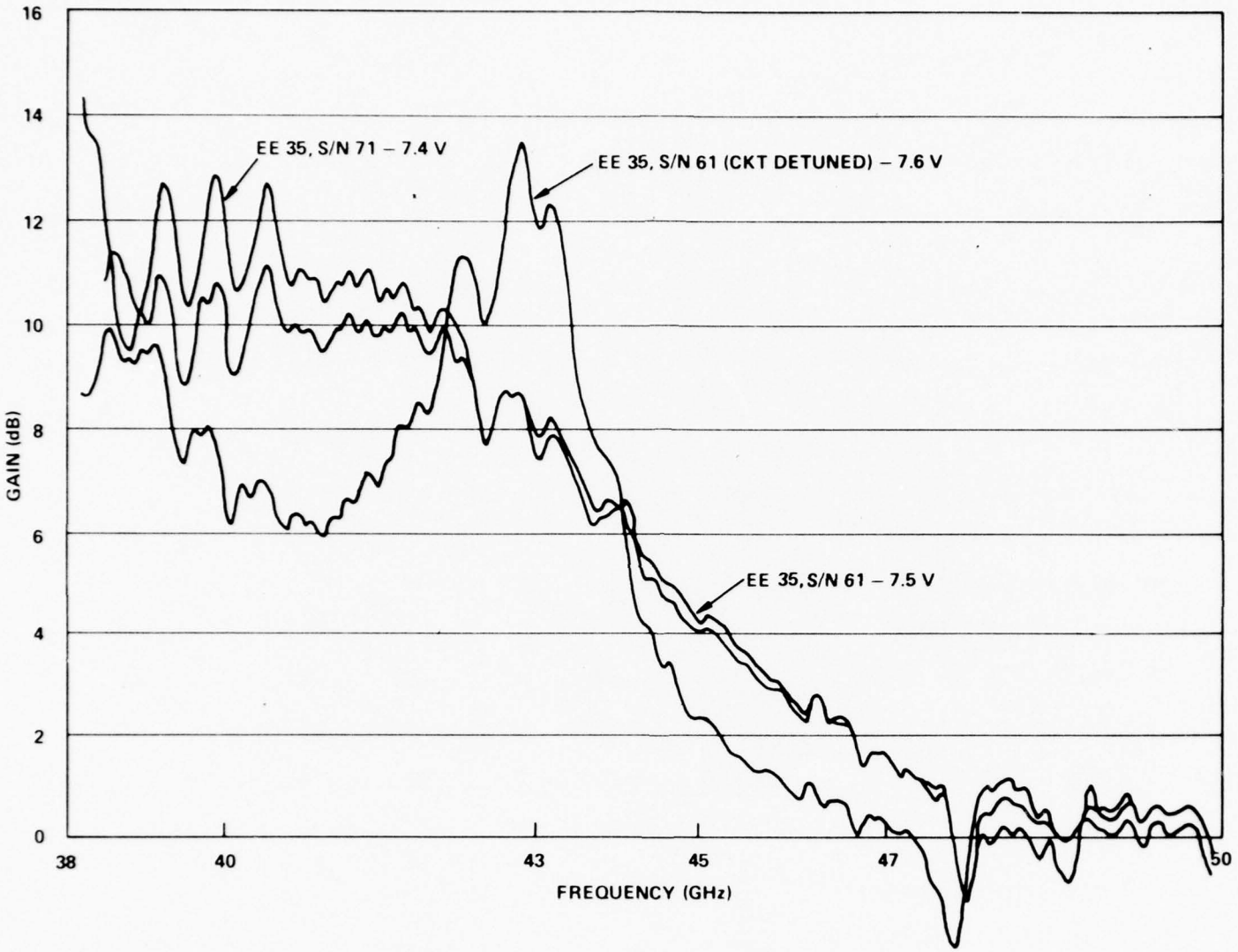


Figure 5.2. Amplifier Gain Responses for Devices from Wafer EE35 at Frequencies Greater than 40 GHz

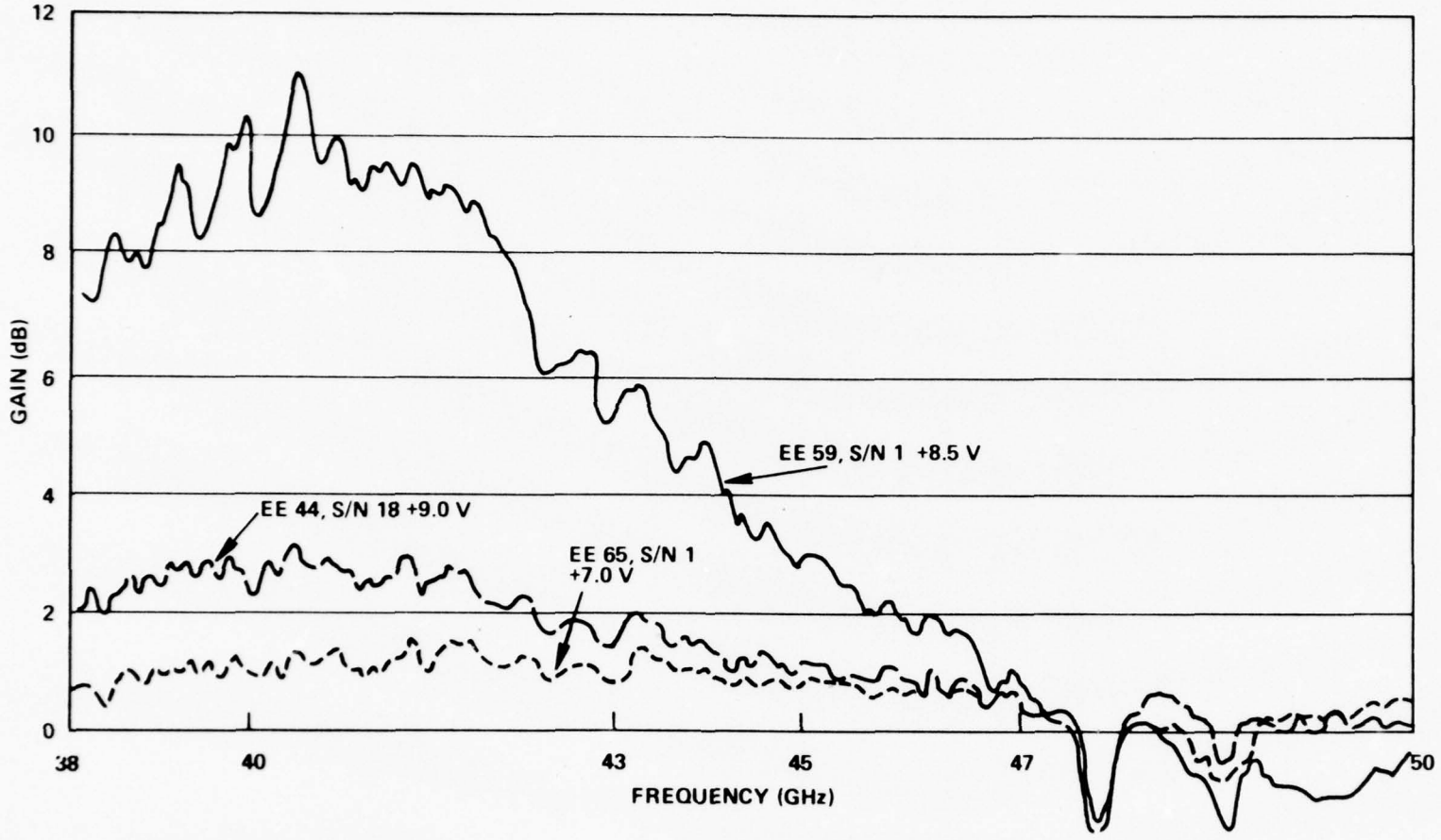


Figure 5.3. Amplifier Gain Responses for Wafers EE59, EE44, and EE65 at Frequencies Greater Than 40 GHz

TABLE 5.3

WAFER SUMMARY

Wafer	$n_o (x10^{15})$ cm^3	l (μm)	$n_o x l$ x 10^{12}	Gain (dB) 38-43 GHz	$\sqrt{V}$ Gain BW
EE35	4.0 - 1.2	4.3	1.12	~ 8	7.1
EE44	1.3 - 0.5	5.7	0.51	~ 1.5	5.2
EE59	3.0	4.5	1.35	~ 5	5.3
EE65	2-3	4.6	1.15	~ 1	5.9

Bandwidth in all cases appears to be circuit limited and, as a higher frequency circuit is utilized, more thorough evaluation of these devices in the 40 - 60 GHz range will be performed. In Ka-band gain in this circuit can extend down as far as 33 GHz. This gives an approximate available bandwidth of 11 GHz, which is similar to bandwidth seen with the 33 GHz amplifier circuit centered in Ka-band.

5.2.3 Low Temperature Measurements

Some thermal problems have been encountered with higher doped oscillator devices on another program, and low temperature measurements were used to evaluate the effects of higher temperature operation. Devices from three wafers, EE66, EE70, and EE71 were checked for gain and noise figure at two different temperatures. The low temperature measurements were made by immersing the amplifier circuit in liquid nitrogen for several minutes with the diode unbiased before testing. Temperatures were on the order of -50° C. For the higher temperature measurements, the diode was operated for several minutes without cooling in a room temperature ambient. It was found that the gain response changed significantly when the devices were cooled. For devices from wafer EE66 and some from EE70 the gain peak shifted up about 3 GHz from 34 GHz to 37 GHz. In most cases peak gain changed by less than 0.5 dB, however. Devices from wafer EE71 and others from EE70 showed a decrease in gain of 2-3 dB with a small increase in frequency of the gain peak (<1 GHz).

Noise figures of devices from EE71 were measured at the two temperatures, using the H-P automatic noise figure meter. The noise figure of the diodes was about 0.4 - 0.6 dB higher when they were cooled. Noise measure was about 0.6 dB higher for the higher gain, higher doped devices and 1.5 - 2 dB higher for the lower gain, lower doped devices when they were cooled.

5.2.4 Reverse Polarity Measurements

Several of the triple-layer contact amplifier wafers were evaluated for gain and noise figure in the reverse (heatsink positive) polarity mode. Of the higher gain wafers, higher noise two-thirds had considerably improved gain levels and the rest showed no change. The lower-doped, lower-gain wafers actually had worse gain performance in some cases with the bias polarity reversed.

5.2.5 Device Reliability

In an effort to establish a meaningful estimate in InP device reliability, several devices from wafer EE71 were placed on dc burn-in. The devices are about 0.35A devices and are operating at +11.5V, their normal operating voltage. The heat sinks are at about 60° C and, with an average measured thermal resistance of 33° C/W, the active layer temperature is about 200° C. Fifteen devices are biased in this life test. There have been several failures, although all but one of these occurred within the first 10 hours after it was put on the life test. The one exception failed after 1003 hours. To date, over 11,500 device hours have been accumulated. This test will be continued in the interim between programs as long as a burn-in rack is available for use.

5.3 A MORE DETAILED LOOK AT SPECIFIC WAFERS

5.3.1 Higher Doped, Higher Noise Wafers

Three wafers grown during the contract period had very good performance in terms of gain levels and negative resistance bandwidths. These wafers were EE33, EE59, and EE70. All had doping levels greater than 2.0×10^{15} cm^{-3}

and lengths greater than 4.5 μm. As a result, noise figures were not low, although they were 5 to 7 dB lower than noise levels measured on similar profile GaAs devices. Noise measures were only slightly higher due to the high gain levels experienced.

In Figures 5.4 and 5.6, plots of gain vs frequency with associated noise figures are shown for devices from these three wafers. The noise figures are given in dB and are the vertical numbers next to the curves. As can be seen from the figures, gains are extremely high, and the devices could be made to oscillate quite easily with slight circuit detuning. Noise figures suffered as a result of the increased doping level. The noise figures for these wafers were comparable to those obtained with GaAs notch devices, although gain levels were slightly higher. Since the main thrust of the program was low noise, further evaluation efforts concentrated on lower doped devices.

Higher doped InP Gunn devices appear to exhibit an increased sensitivity to bias voltage changes, as evidenced by changes in gain. Figure 5.7 presents a typical gain response of a lower frequency amplifier as a function of bias voltage. Shifts of the reactive portion of the device impedance appear to be more in line with those observed for GaAs devices, as there is little frequency shift of the gain passband as bias voltage is varied. The InP devices measured typically exhibited an 11% change in negative resistance for a 0.1 V change in bias near the maximum negative resistance point. GaAs devices with similar profiles exhibited a 3% change when measured in the same manner. This sensitivity does indicate more stringent requirements on power supply noise levels in view of the possible higher AM conversion in oscillator and noise figure degradation in amplifier applications.

5.3.2 Lower Doped, Lower Noise Wafers

Very low noise performance was obtained with three wafers having lower doping levels. These three are EE44, 66 and 71. Doping levels for these

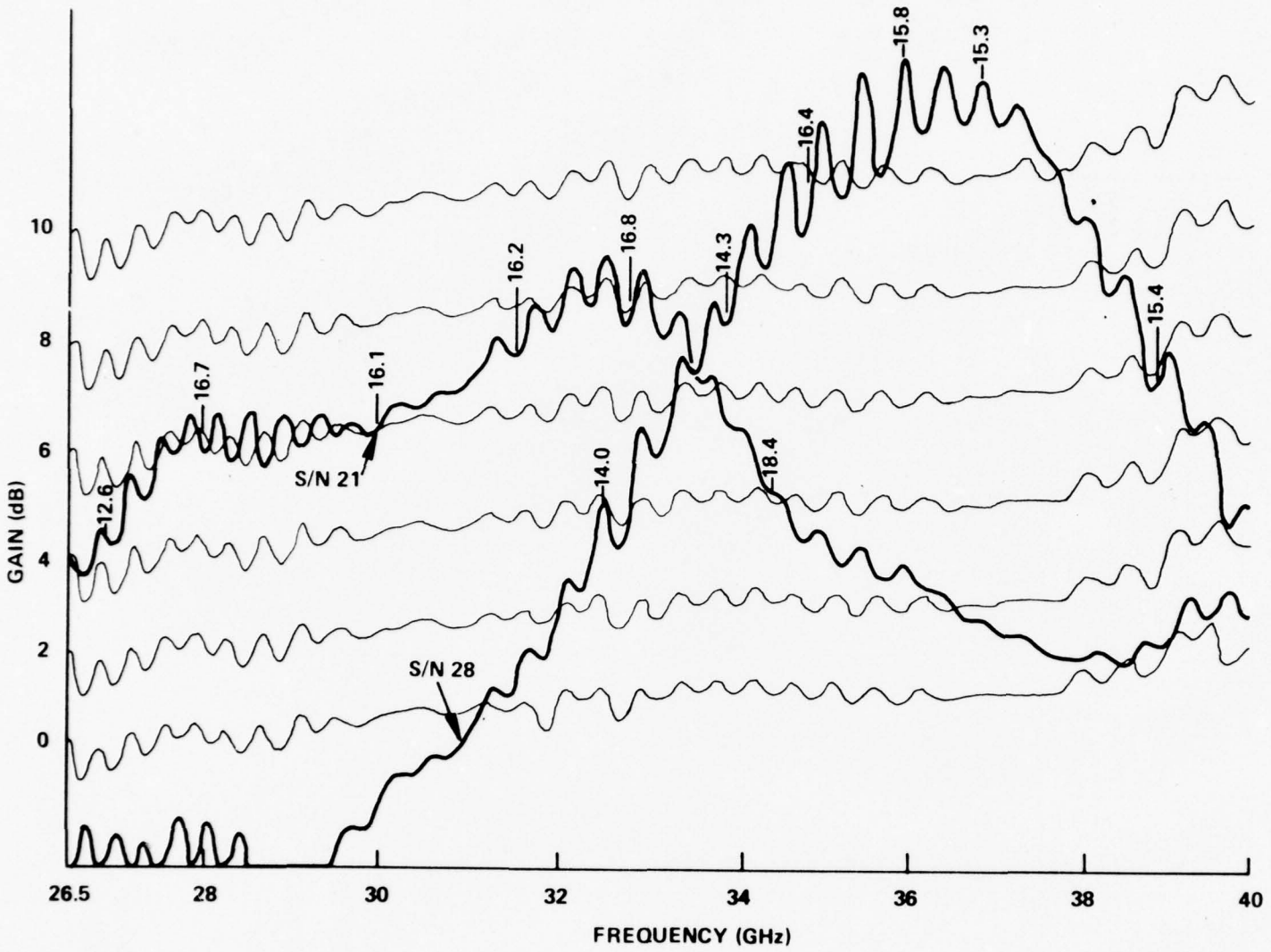


Figure 5.4. Upper and Lower Frequency Band Amplifier Gain Responses for Devices from Wafer EE33. The vertical numbers are device noise figures in dB.

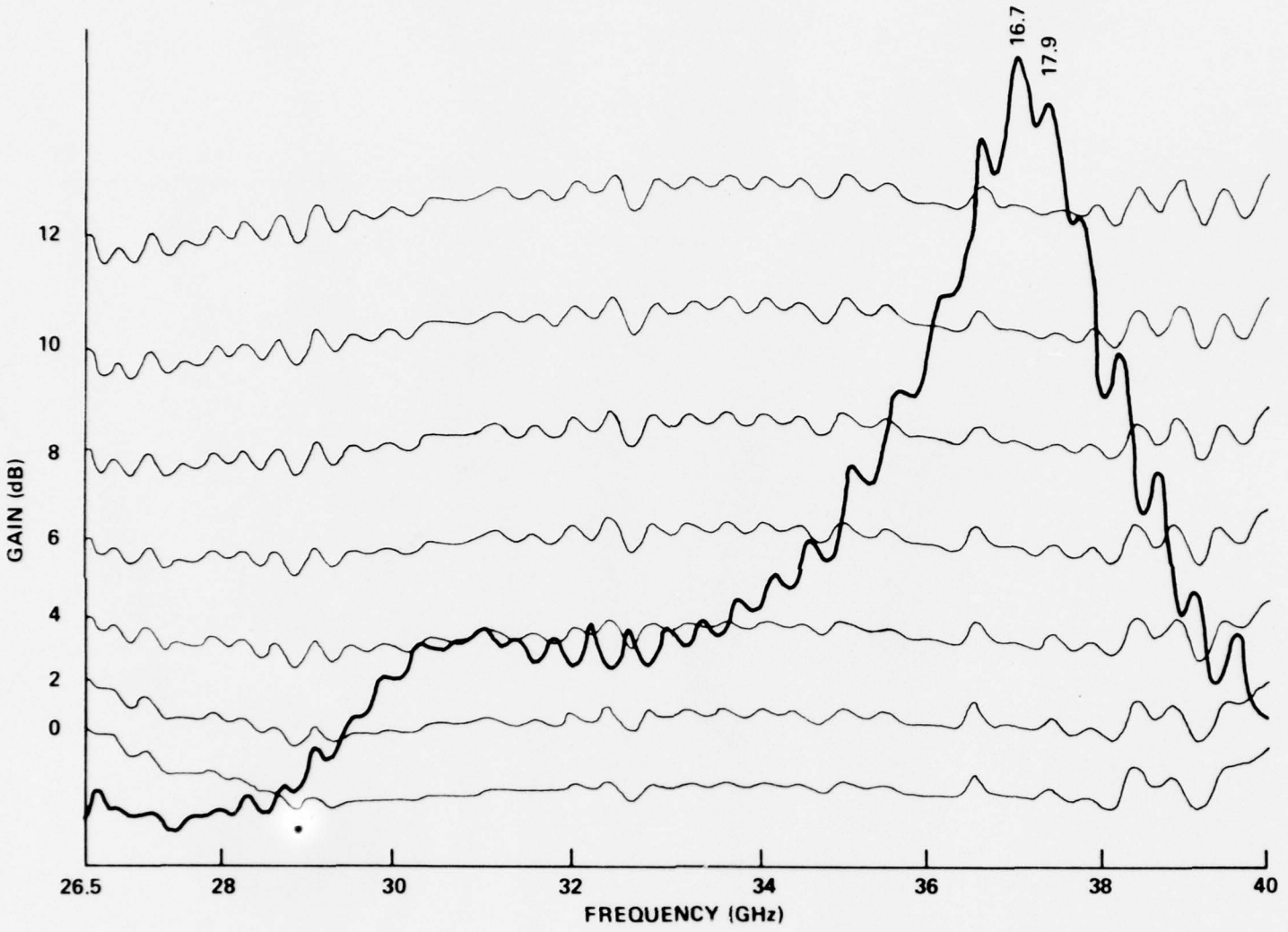


Figure 5.5. Typical Amplifier Gain Response for a Device from Wafer EE59. Vertical numbers are device noise figures in dB.

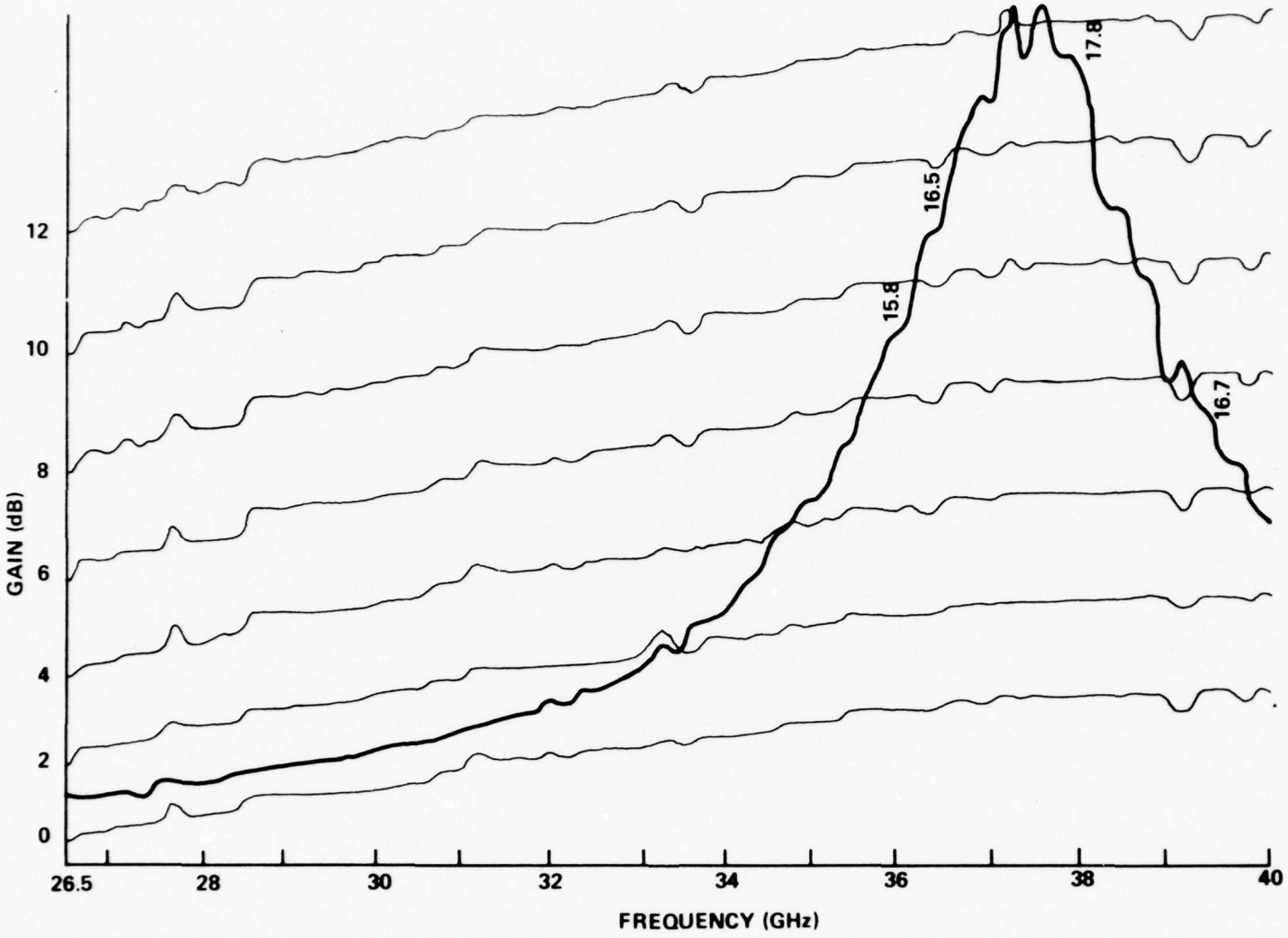


Figure 5.6. Amplifier Gain Response for a Device from Wafer EE70. Vertical numbers are device noise figures in dB.

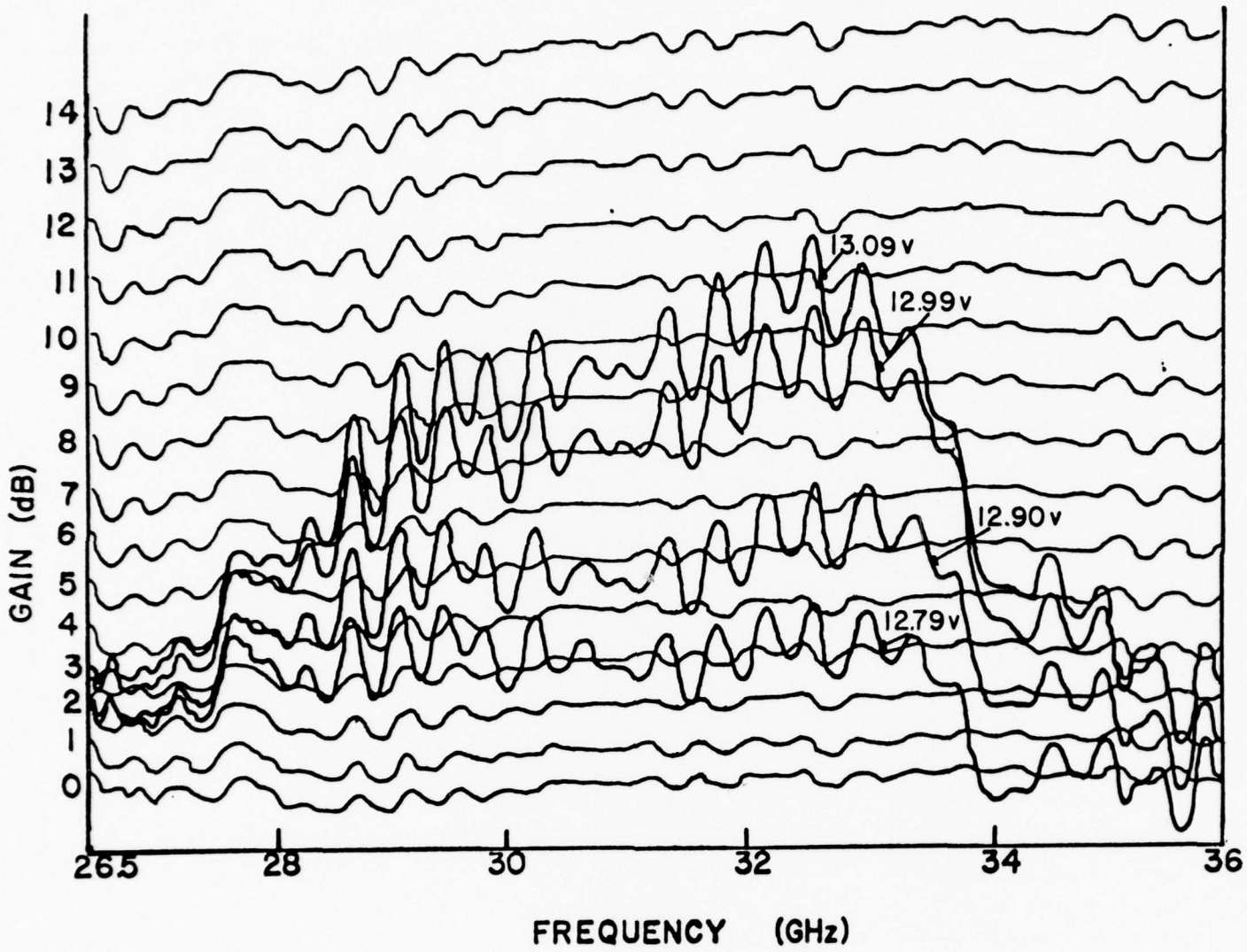


Figure 5.7. Amplifier Gain Response as a Function of Bias Voltage

devices are all below 1.0×10^{15}, although they do have sloped profiles. Lengths are medium to long covering the 4 to 6 μm range. As a result of the low doping levels the negative resistance was correspondingly lower, as were the gain levels. Wide band gains were typically one to two dB, although wafer 71 showed higher gains in the 3 to 6 dB range.

In order to obtain meaningful noise figure information, a narrowband circuit was utilized to give higher gain levels. Figures 5.8 and 5.9 present gain pictures for devices from wafers 44 and 66. Again, the vertical numbers represent device noise figures. In Figure 5.8 we can see that the noise figures decrease slightly as the bias voltage is increased.

Devices from wafer EE71 (one of the later series) have provided exceptional performance in wideband amplifier circuits. Judging by the doping level, wideband gains were higher than anticipated. Typical gain responses in the 38 GHz half-band amplifier circuit are shown in Figure 5.10 for several devices from the wafer. These responses were measured with the amplifier on a circulator, but circulator insertion losses are not included in the gain values. Operating voltages are shown on the graph. Operating currents are in the 0.25 to 0.4 A range. The devices would also operate in the 33 GHz circuit, but at somewhat reduced gain levels and higher operating voltages. If the voltages were raised further to check operation in the lower half-band amplifier circuit, gain was either very low over the frequency range (<1 dB) or the devices failed.

Noise figures on several devices from this wafer were measured by several methods and gave numbers in the 8 to 12 dB range, depending upon the method used. Table 5.4 presents a summary of noise figures for the devices as measured with three configurations.

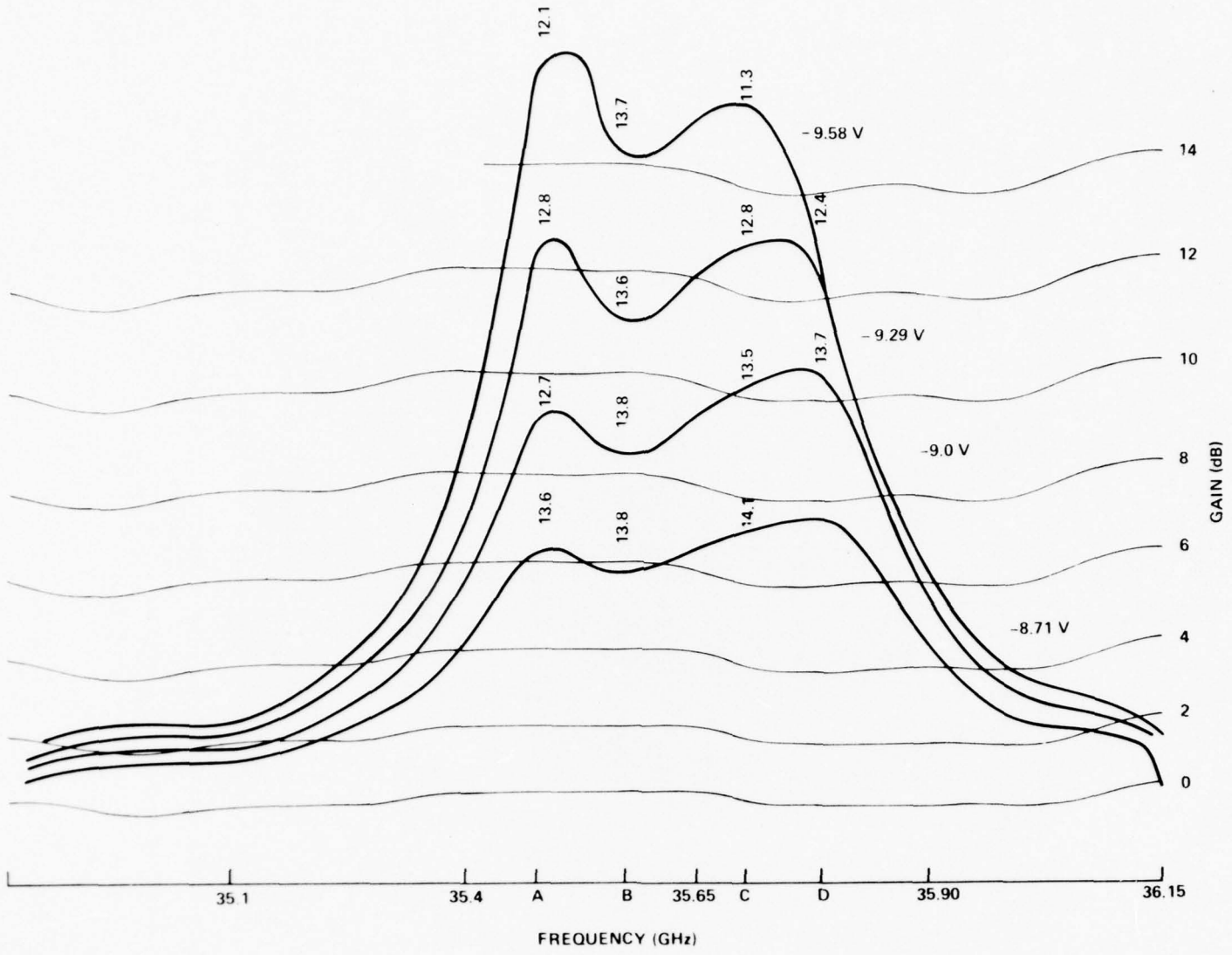


Figure 5.8. Narrowband Amplifier Response for Wafer EE44

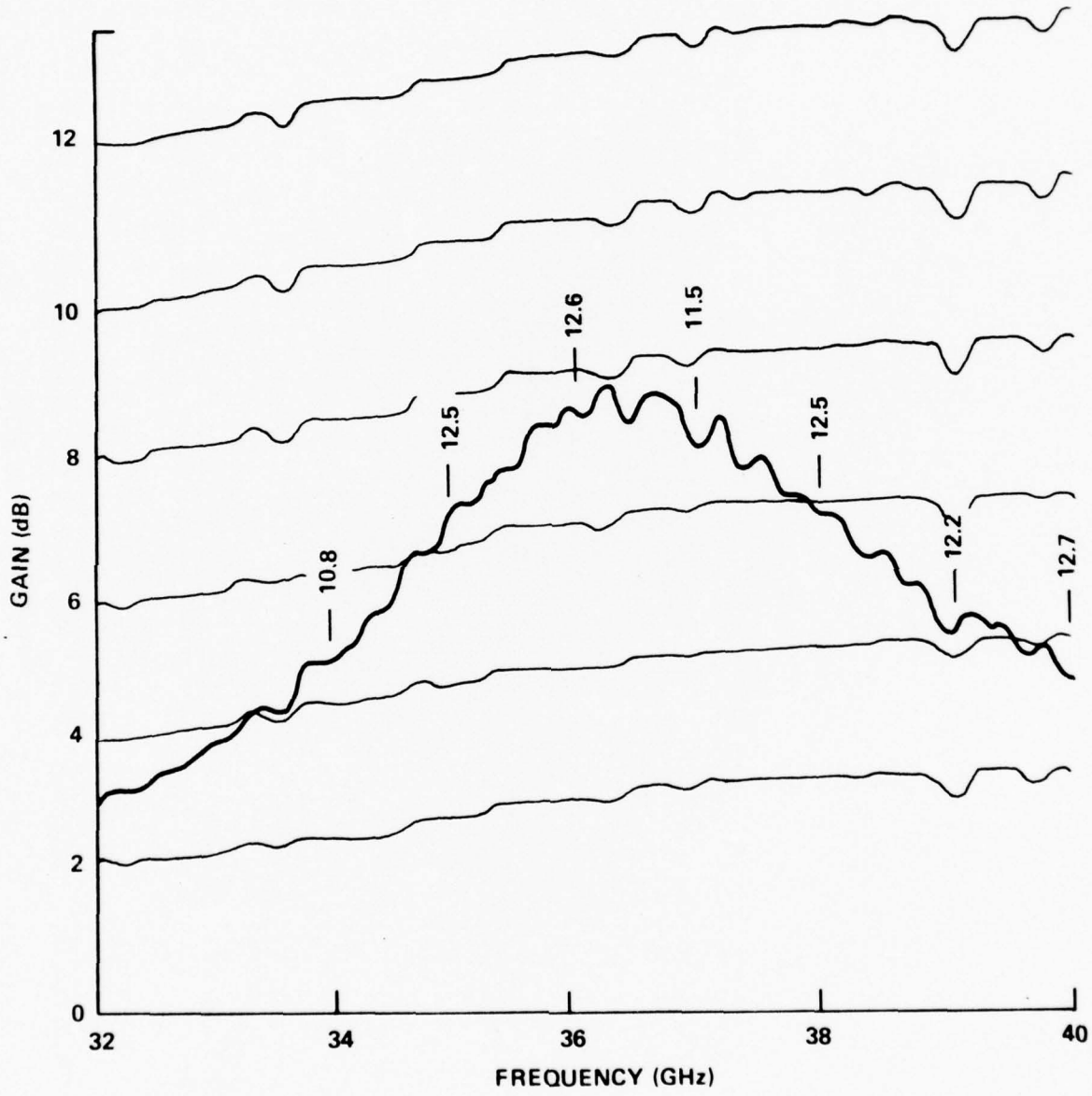


Figure 5.9. Typical Gain Response of a Device from Wafer EE66. Vertical numbers are device noise figures in dB.

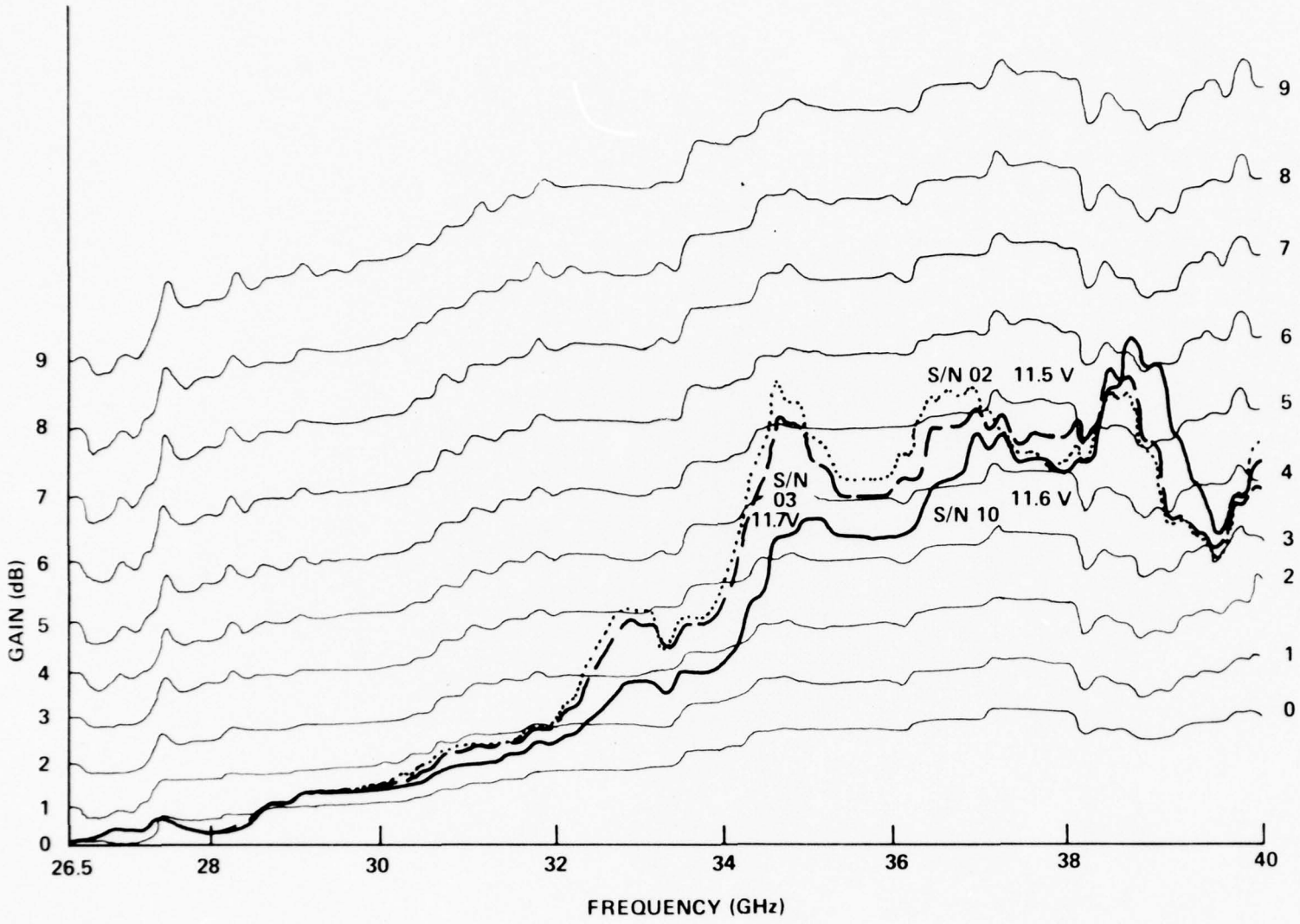


Figure 5.10. Typical Amplifier Responses for Devices from Wafer EE71. (Amplifier measured on circulator.)

TABLE 5.4

34 to 40 GHz DEVICE NOISE FIGURES - WAFER EE71

NOISE FIGURES - dB (Noise Measures Below in Parentheses)

DEVICE S/N	MANUAL HP METER	AUTOMATIC HP METER	AUTOMATIC AIL METER
2	7.5 - 11.8 (10.9 - 14.0)	6.8 - 9.3 (9.3 - 13.6)	9.6 - 10.7 (11.2 - 12.9)
3	7.3 - 11.7 (8.6 - 13.7)	6.7 - 7.8 (9.6 - 14.6)	
5	6.6 - 9.2 (9.7 - 12.7)	6.4 - 8.1 (10.2 - 13.8)	8.3 - 10.0 (12.1 - 14.5)
10			9.0 - 10.0 (10.8 - 12.0)
11			8.2 - 9.3 (10.7 - 11.8)

The numbers represent device values - contributions from receiver noise and circulator losses have been subtracted where applicable. The range of noise measure is shown in parentheses under noise figure values.

The discrepancies between values taken with the two instruments in the automatic mode are reduced somewhat if a narrower frequency region is considered where InP amplifier gain is higher. In this region, the AIL meter has a higher reading, by 1.27 dB, for several devices (1.27 dB is the average difference in noise figure values for the same device over several frequencies). Approximately a 1 dB difference in noise figure values has been previously noted during lower frequency (X-band) noise measurements using the two meters. Part of the discrepancy is attributable to the fact that the HP meter is calibrated for a noise tube with a fixed noise ratio which is approximately 1 dB below that actually used.

Under any circumstances, noise figures well below 10 dB have been demonstrated in this laboratory with accompanying usable wideband gain levels of 3 to 6 dB in the 34 to 40 GHz frequency range.

Compression measurements were made on devices from wafer EE71 and considerably improved compression performance was noted over previous measurements on early wafers. In amplifier circuits with gains in the 4 to 5 dB range, the 1 dB compression point was at greater than + 3 dBm input power (the limit of our measurement equipment capability). In a 7 dB gain amplifier, a drop to 6 dB gain occurred with + 1.5 dBm input power. In all cases, smooth compression characteristics with no apparent gain expansion were noted.

5.3.3 Device Impedance Measurements

Plotted in the next several figures is the negative of the terminal impedance for devices from several of the better Inl ers measured in the 33 to 40 GHz range. Plotted on the Smith chart in Figure 5.11 are device curves for GaAs devices with both flat and cathode notch doping profiles. Also plotted in Figure 5.13 is the measured circuit impedance for the 38 GHz half band amplifier circuit. These curves represent averages of device data taken for several devices from each wafer. Variations from device to device in a given wafer are predominantly reactive in nature, although some wafers experienced greater variations in reactances. Typical reactance spreads are 2 to 10 ohms. Real part variations up to 50% are also typical. A summary of average device Q for the wafers measured is given in Table 5.5. Also shown is the real part and the change in real part of the device impedance across the frequency range from which the device Q was calculated.

The InP devices exhibit higher Q's than GaAs devices and as a result appear to have narrower bandwidths when measured in GaAs-type amplifier circuits. The smaller change in real part of the device impedance makes device matching somewhat easier, however. Also evident from the table and Smith charts is that device Q increases as doping decreases, primarily due to the decrease in negative resistance magnitude. One interesting feature that is displayed by devices from the

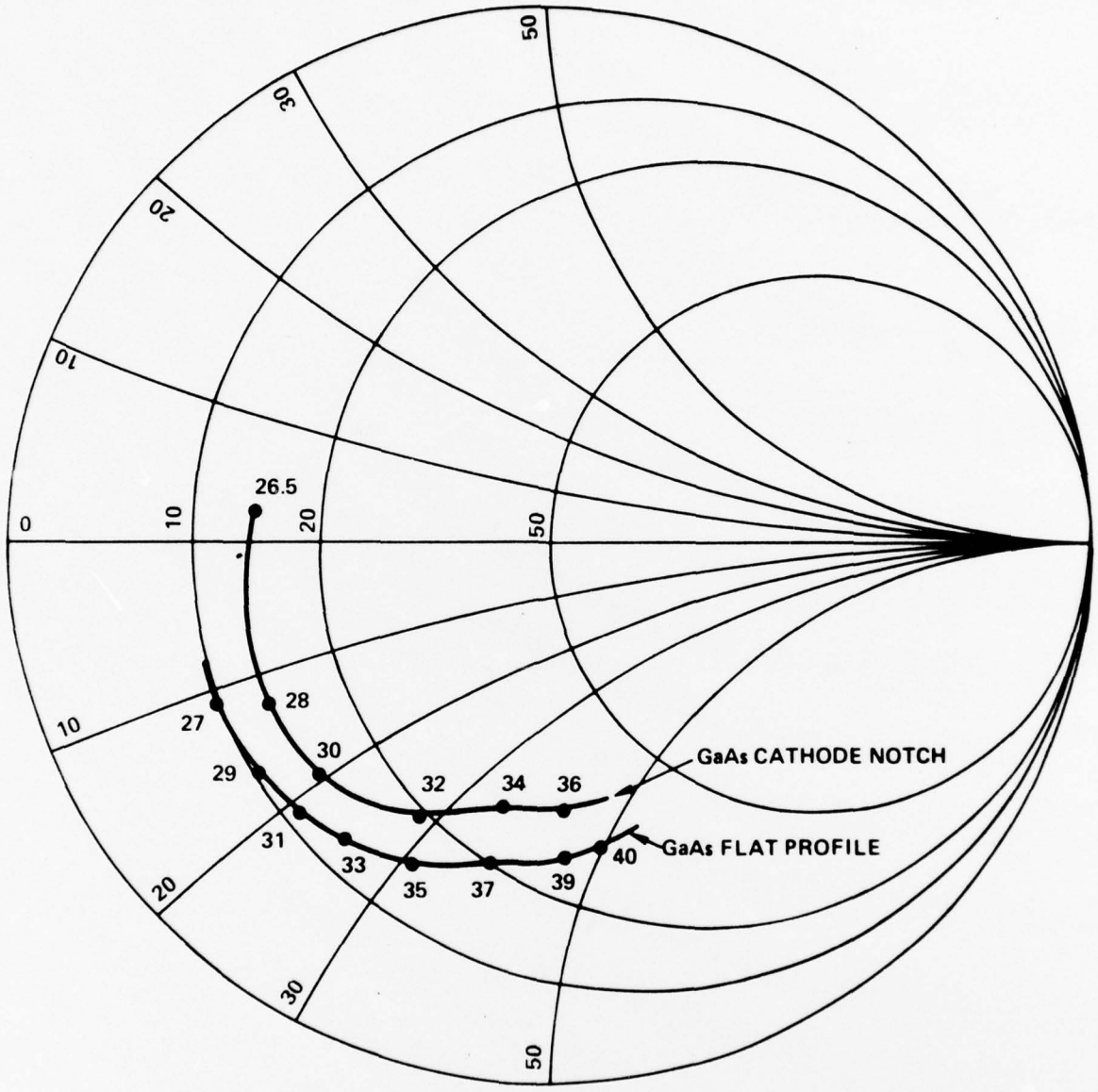


Figure 5.11. Negative of the Terminal Impedance for GaAs Flat and Cathode Notch Gunn Devices

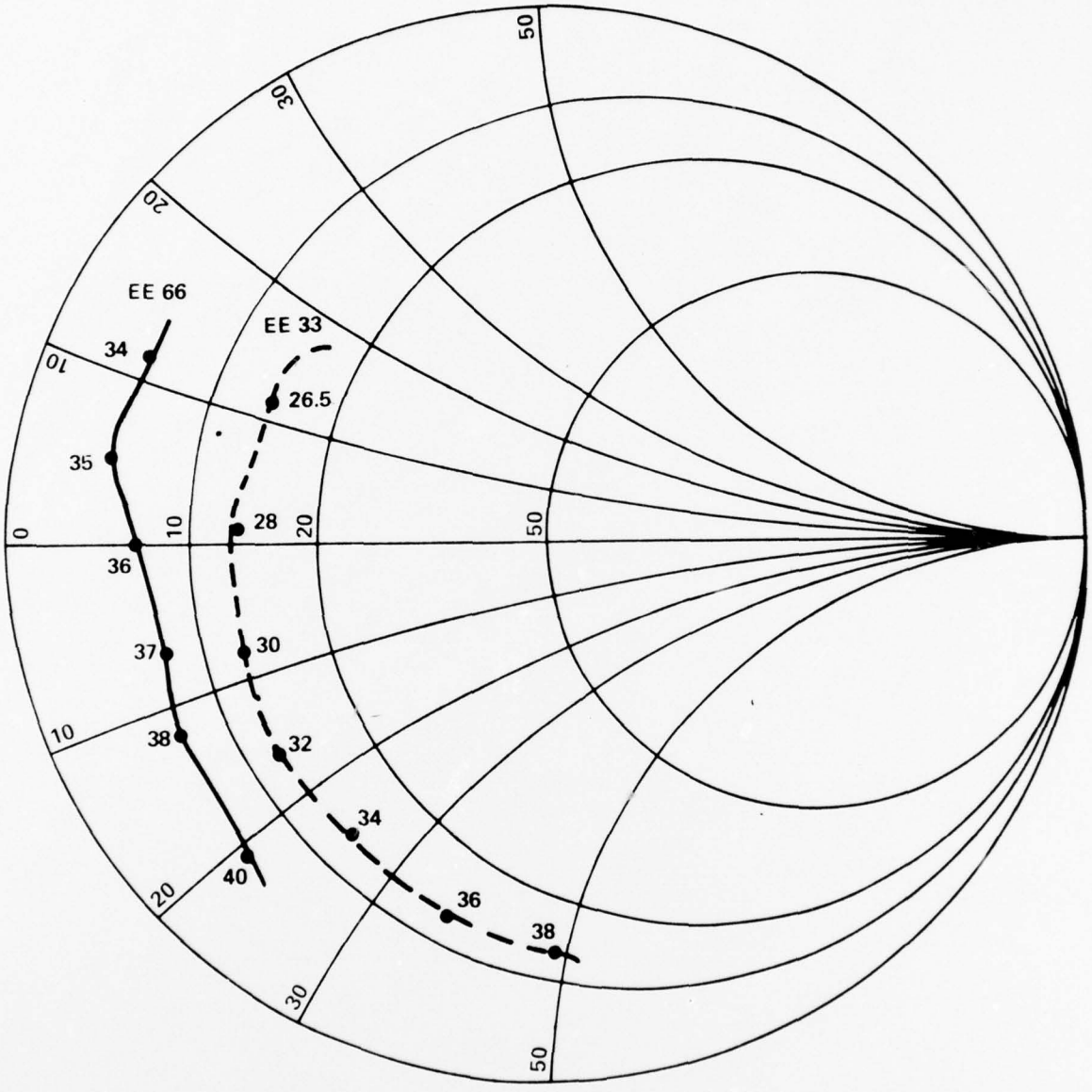


Figure 5.12. Negative of the Terminal Impedance for Devices from InP Wafers EE33 and EE66.

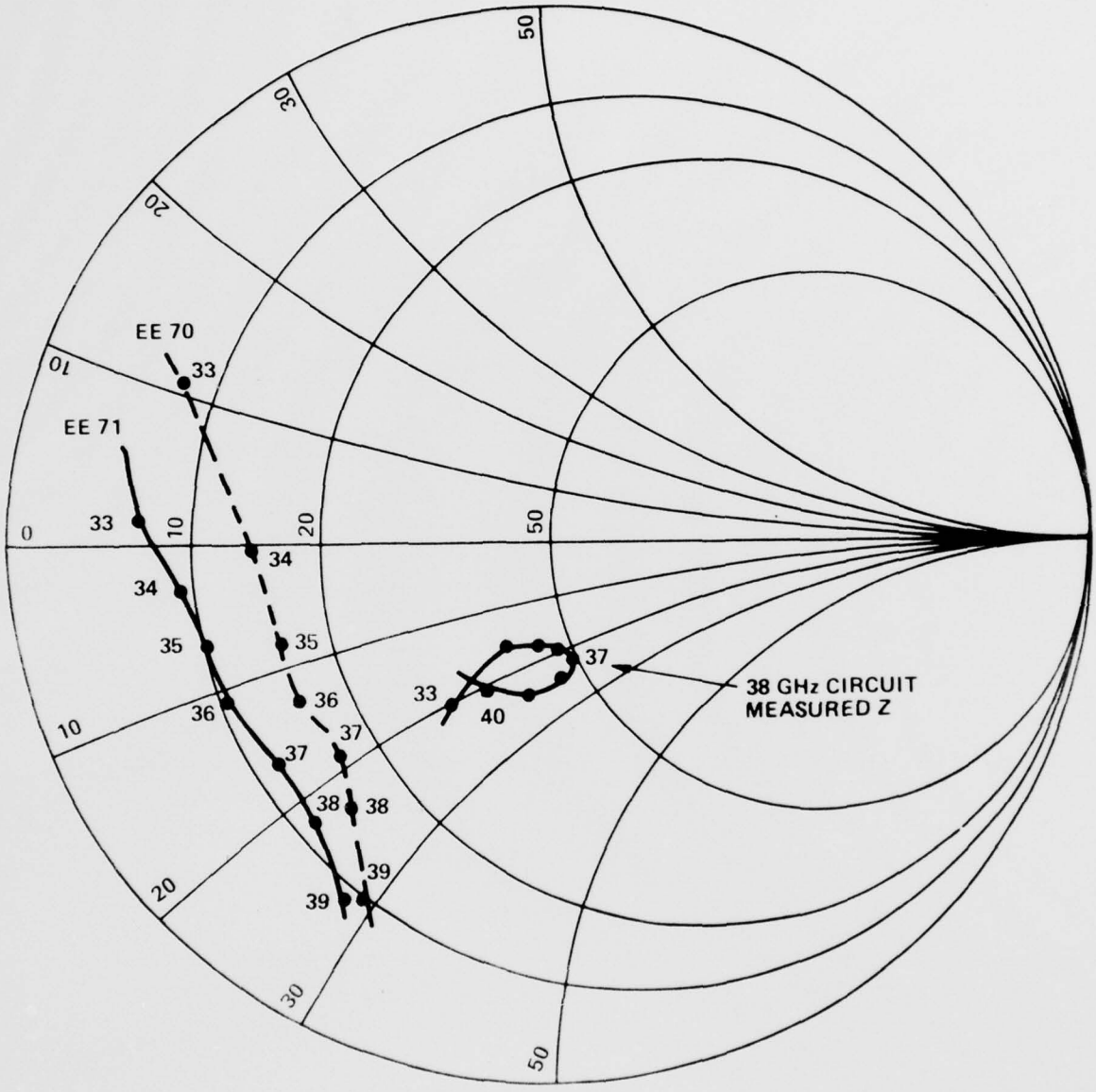


Figure 5.13. Negative of the Terminal Impedance for Devices from InP Wafers EE70 and EE71. Also plotted is the 38 GHz circuit impedance.

TABLE 5.5

DEVICE Q FOR SEVERAL InP WAFERS WITH TWO GaAs DEVICE TYPES FOR COMPARISON $\left[Q = \frac{\Delta x}{\Delta f} \quad \frac{fo}{2R}\right]$

WAFERS	$-\overline{R}(\Omega)$	$\Delta R(\Omega)$	Q
33	13	$\pm$ 1.5	6.5
66	6	$\pm$ 1.5	16.7
70	15	$\pm$ 4.5	7.3
71	10	$\pm$ 2.5	9.0
GaAs Flat	18	$\pm$ 10	2.8
GaAs Notch	18	$\pm$ 9.5	4.4

later InP wafers is that the packaged device is resonant at much higher frequencies than either GaAs or early InP. The InP devices resonate in mid to upper Ka-band, whereas the GaAs devices resonate in K-band usually about 23 GHz. This is as expected because of the increased physical length of the device (due to higher electron velocity) and resulting decreased capacitance.

In Figure 5.14, amplifier gains are calculated based upon measured circuit and device impedances using the following equation for reflection coefficient:

$$\Gamma_A = \frac{\left|Z_c - Z_D^*\right|}{\left|Z_c + Z_D\right|}$$

The magnitudes and frequency ranges correlate quite well with those observed and reported on for similar circuit types.

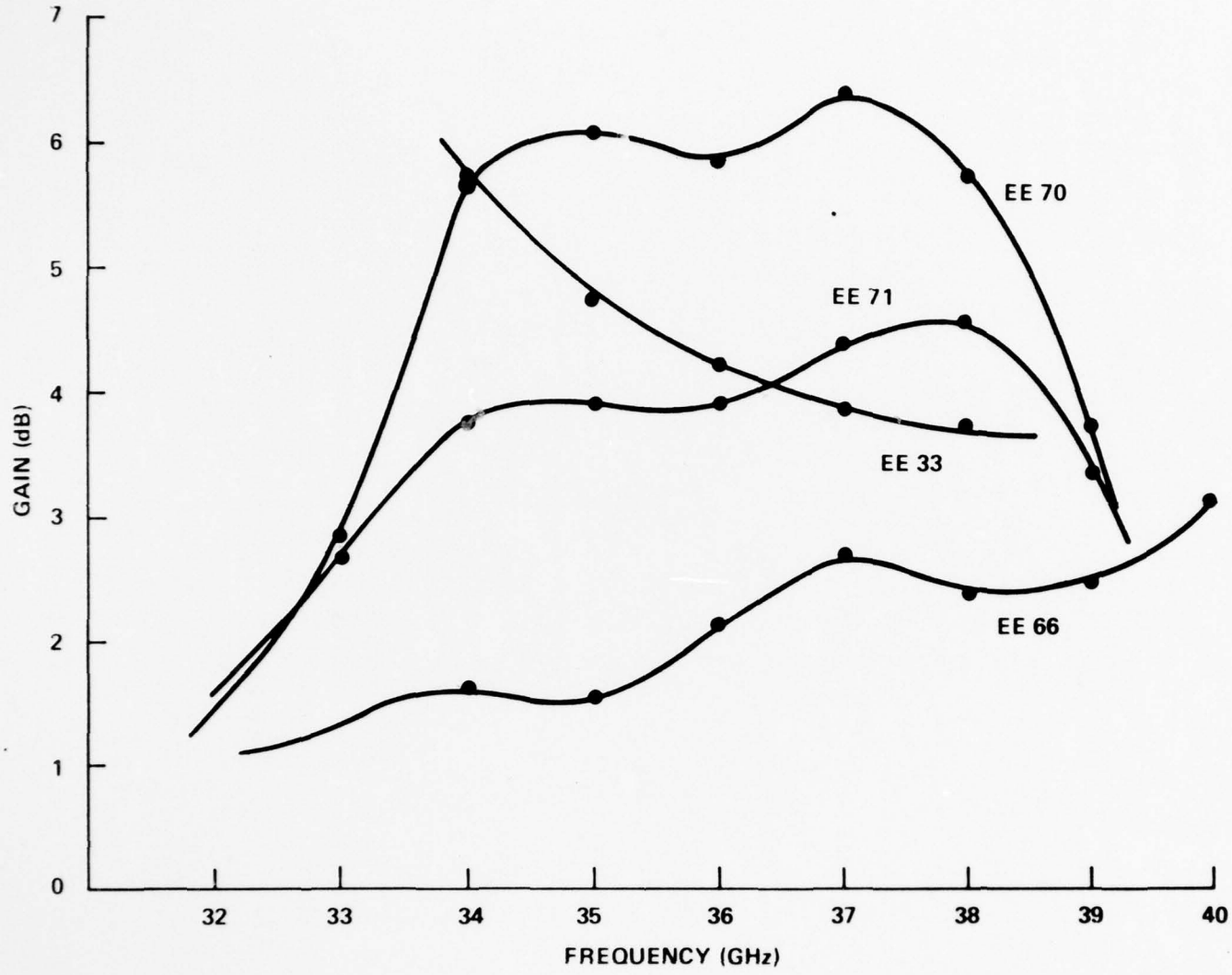


Figure 5.14. Calculated Gains for Various InP Wafers Using Measured Device and 38 GHz Circuit Impedance Data

6. AMPLIFIER CIRCUIT DEVELOPMENT

6.1 GENERAL CIRCUIT DISCUSSION

As described briefly in a previous section and shown in Figure 6.1, the amplifier circuits utilized during this program were of the coaxial/waveguide hybrid type. A standard circuit design at 33 GHz forms the basis for scaling circuit dimensions to other center frequencies in and beyond Ka-band. Dimension of both the inner and outer coaxial conductors, as well as waveguide opening size and depth, are critical for proper operation.

Generally, coax line impedance as determined by the center conductor diameter sets the gain level while the waveguide impedance transformer ratio and electrical length between the full height output waveguide and the coax line determines the bandwidth. Also extremely important is the area of the coaxial line immediately surrounding the diode. Recessing the 0.120" diameter diode flange into the heat sink greatly reduces the mounting inductance and enables easier matching for wide band operation. The waveguide to TEM transformation takes place near one end of the coaxial line and therefore magnetic coupling predominates.

Circuits are available to cover all portions of the 26.5 to 40 GHz band, but none of the wafers grown operated in the 26.5 to 32 GHz portion of the band with the exception of wafer EE33.

6.2 HYBRID COUPLED AMPLIFIER MEASUREMENTS

As InP Gunn devices are considered for use in higher frequency bands (above 40 GHz) as reflection amplifiers, the problem of successfully coupling the rf signal into and out of the amplifier in a nonreciprocal manner becomes more difficult. Ferrite circulator limitations, specifically the $4\pi M_s$ of the ferrite material, limit fundamental mode low loss operation to frequencies below 40 GHz. Circulators with up to 8% bandwidths and reasonable return loss and isolation performance are available as laboratory models through 60 GHz. For wider band coverages considerable development effort must be expended or alternate approaches must be explored.

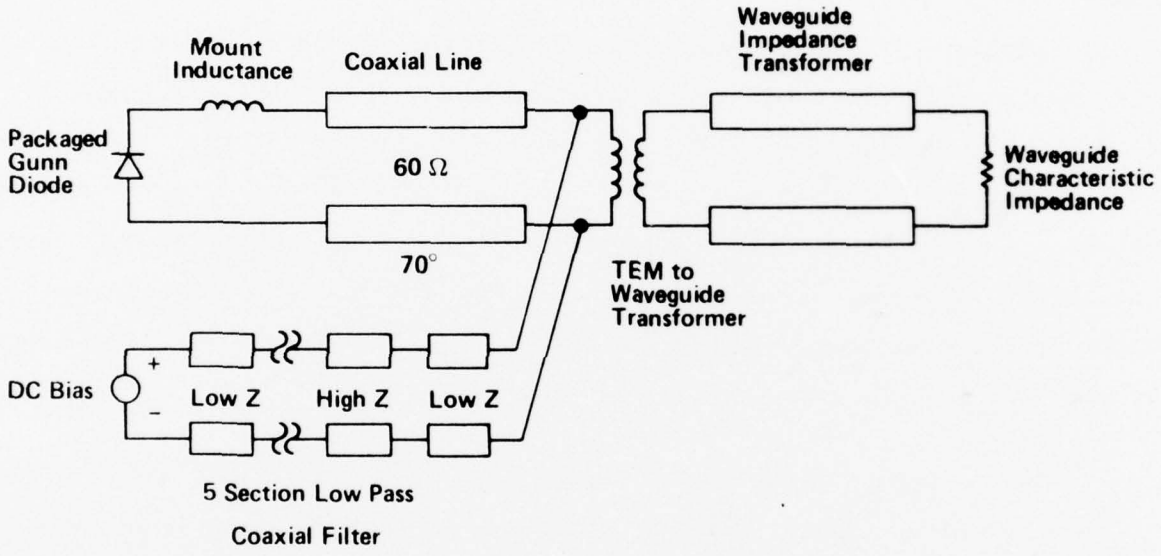


Figure 6.1. Amplifier Circuit Schematic

One approach that was evaluated in upper Ka-band was that of using a 3 dB hybrid coupler. This waveguide unit is commercially available and is designed to cover the entire band. Full band performance levels are: better than 14 dB return loss over the band (better than 16 dB from 28 to 38 GHz), and less than one dB of insertion loss between the input port and the output port with both amplifier ports shorted. Two amplifiers were measured on the reflectometer setup and were slightly adjusted to be as identical as possible in terms of gain level and frequency response. Phase shift was not measured. The two amplifier circuit responses are shown in Figure 6.2.

The two circuits were then placed on ports A and C of the 3 dB hybrid coupler. The output at port D due to input applied at port B is shown in Figure 6.3. As can be seen from the figure, the overall gain level looks identical to either one of the individual stage amplifiers in terms of both bandwidth and gain level. Unfortunately, the return loss measured at port B was quite low, implying that the isolation with biased amplifiers in place of short circuits is not good. It is apparently not sufficient to merely tune the amplifiers for identical gain and bandwidth values, but the relative phase change must also be taken into account to achieve high isolation as well as good gain response from this hybrid coupled approach.

6.3 KA-BAND NETWORK ANALYZER

A network analyzer for the 26.5-40 GHz band was assembled for diode impedance characterization. All small signal impedance measurements of Ka-band devices were made using a slotted line, which can lead to inaccuracies due to the probe-induced perturbations in the fields in the waveguide. Also, it is a time-consuming process, as all measurements must be done point by point in frequency.

As a result, a Hewlett-Packward R8747A transmission and reflection test unit was added to our standard network analyzer. This test unit mixes a local oscillator and a swept source to convert to a frequency in the normal operating range of the network analyzer.

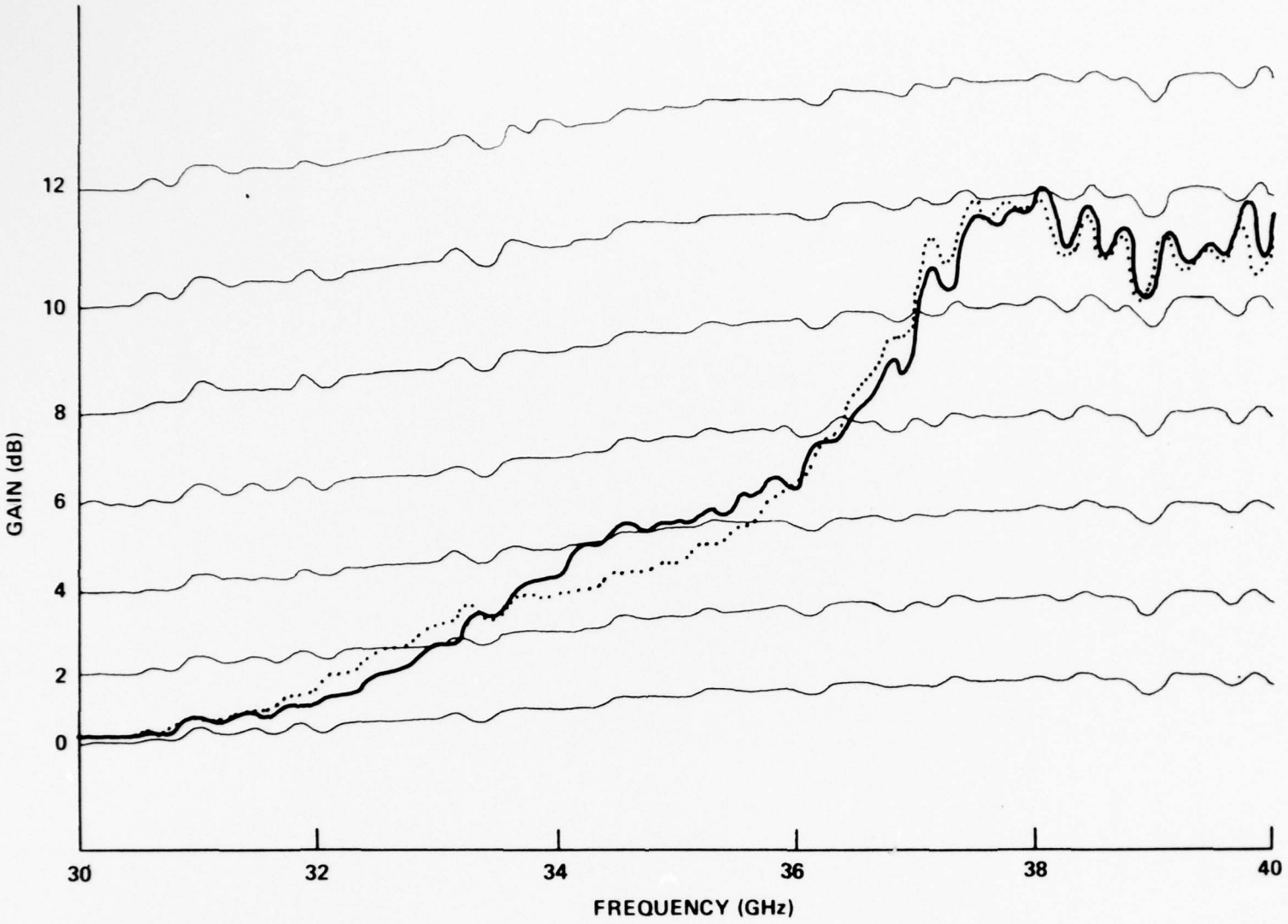


Figure 6.2. Individual Matched, 37 GHz Amplifier Circuit Responses

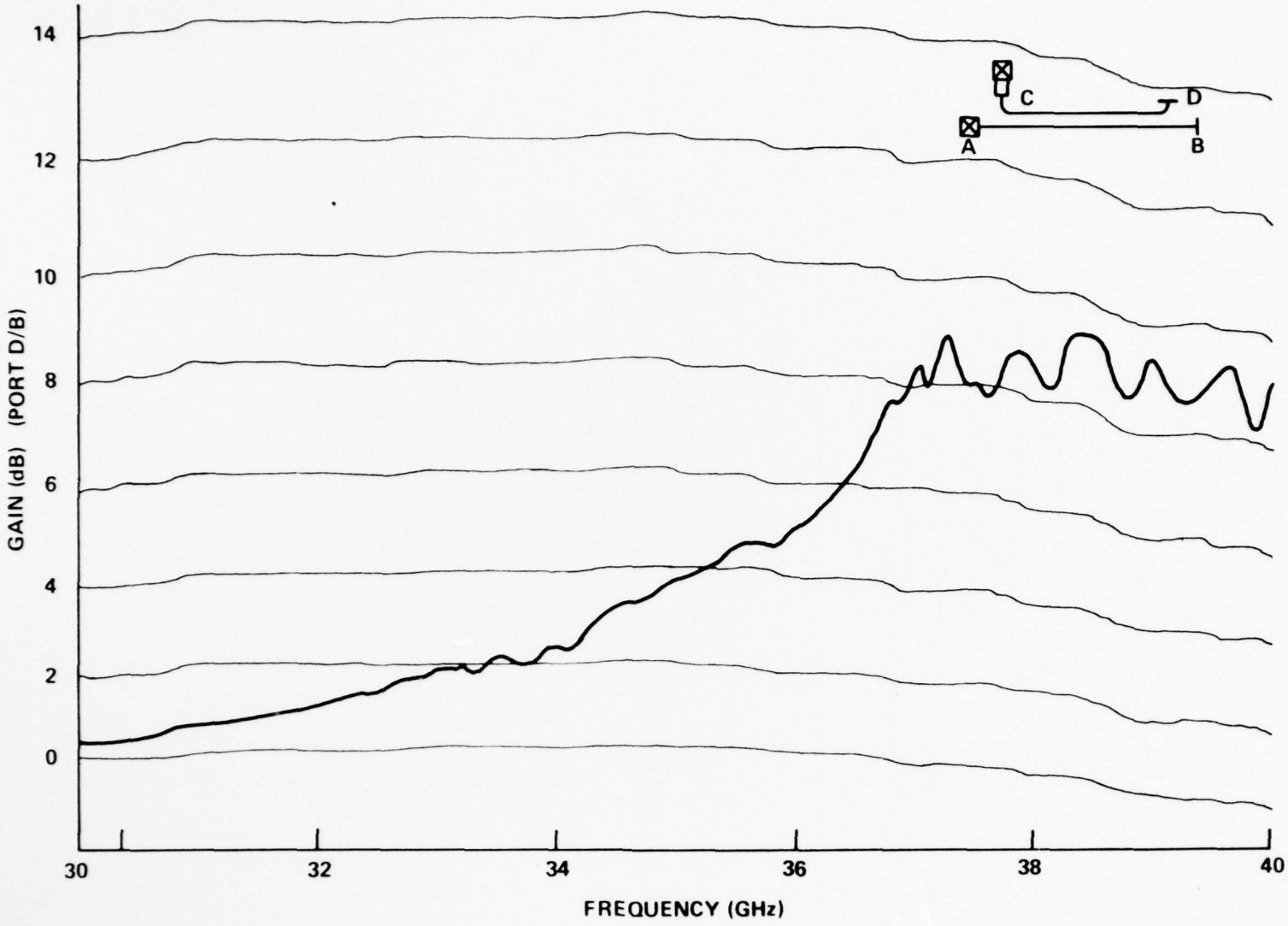


Figure 6.3. 3 dB Hybrid Coupled Amplifier Gain Response.
Output measured at Port D, input applied at Port B.

The Gunn devices are characterized in a normal amplifier circuit. The diode is placed at the end of a coaxial line which is coupled to the waveguide with an iris. As a result, "real time" device impedance measurements on the polar display are not possible. The circuit must be fully characterized to calculate the actual device impedance from the measured impedances. An HP-9821 desk-top calculator is used to control the swept frequency and calculate through the circuit Z-matrix to the diode reference plane. This procedure is similar to the procedure used with the slotted line technique. The use of the calculator to control the signal frequency and read data, plus perform calculations automatically, greatly increases accuracy and decreases time required for the measurement.

Equipment difficulties with the BWO sweeper plug-ins precluded our obtaining meaningful diode characterization results. Proper network analyzer operation has been verified in the manual mode and the feasibility of using the calculator to accurately control frequency in this millimeter wave band has been demonstrated. Efforts will continue during the between-program period to make this system fully operational.

7. CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE STUDY

It has been verified during the course of this one-year program that InP Gunn devices offer significant advantages over GaAs devices in noise figure performance as wideband amplifiers. Noise figures up to 13 dB lower than flat profile and 7 dB lower than cathode notch profile GaAs devices have been demonstrated. Additionally, as solid state components, they will offer significant advantages over conventional means of providing wideband, high gain, low noise amplification in the millimeter wave frequency ranges. This is the main reason for the continuing interest in solid state devices of this type. The noise figures observed during the course of this work are at least 7 dB lower than those attainable with standard traveling wave tubes with the additional advantages of longer life and much simpler power supply design.

Several tasks remain that would further enhance the attractiveness of this new device. There should be continued optimization of device active layer doping and length for lower noise and maximum gain bandwidth product. This effort should include development of material growth and device designs to provide a cathode notch device structure. Another task is the completion of the integral heat sink or plated heat sink process development and InP metalization system to provide better control over the device thermal properties and to maximize device yield.

Efforts should be made to extend the device operating ranges into the 40 to 60 GHz frequency band. Noise figure and lifetime advantages of InP Gunn devices are even more attractive in this millimeter wave frequency range.

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